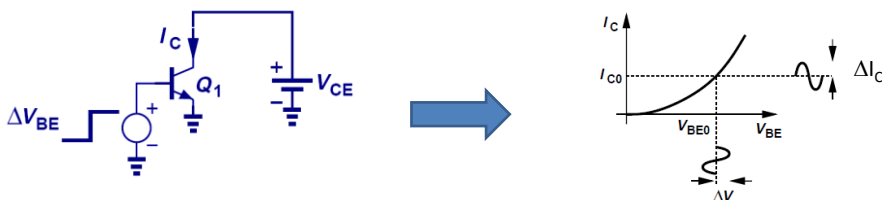


EE 530 Eletrônica Básica I

Transistores Bipolares de Junção

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Transcondutância



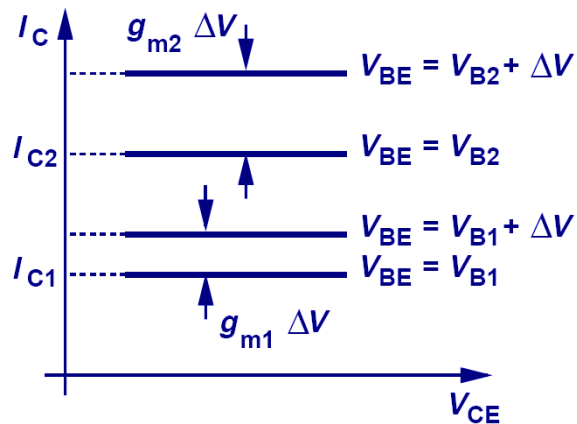
$$g_m = \Delta I_C / \Delta V_{BE} \quad \longrightarrow \quad g_m = \frac{dI_C}{dV_{BE}}$$

$$g_m = \frac{d}{dV_{BE}} \left(I_S \exp \frac{V_{BE}}{V_T} \right) = \frac{1}{V_T} I_S \exp \frac{V_{BE}}{V_T}$$

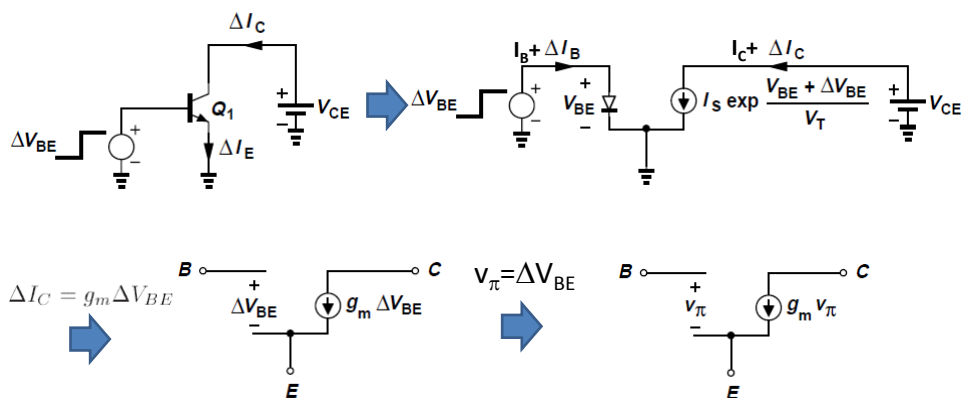
$$g_m = \frac{I_C}{V_T}$$

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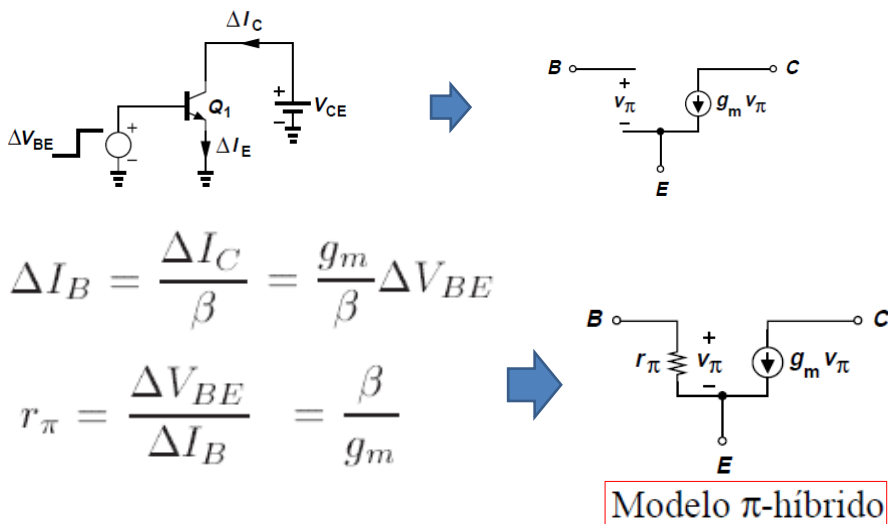
Transcondutância



Modelo de pequenos sinais

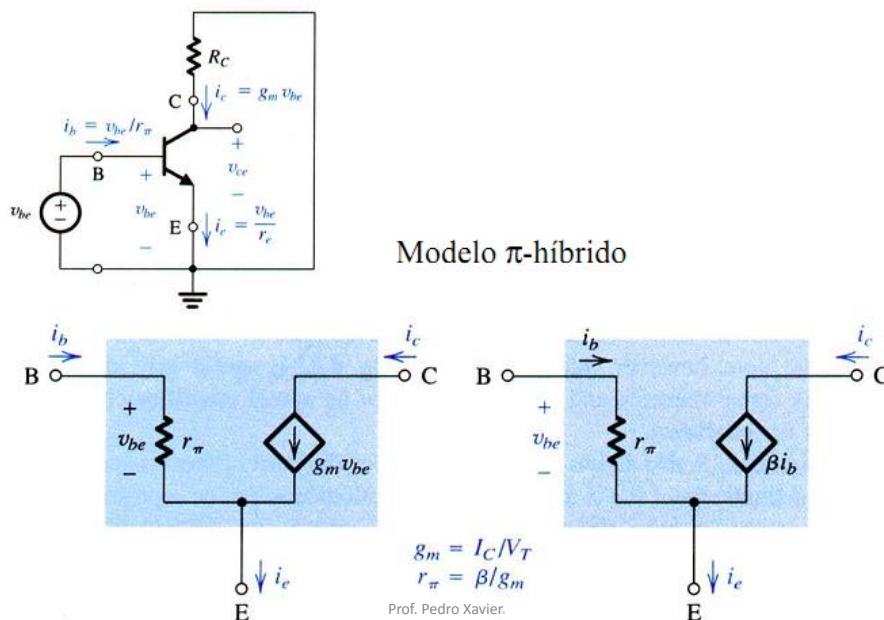


Modelo de pequenos sinais



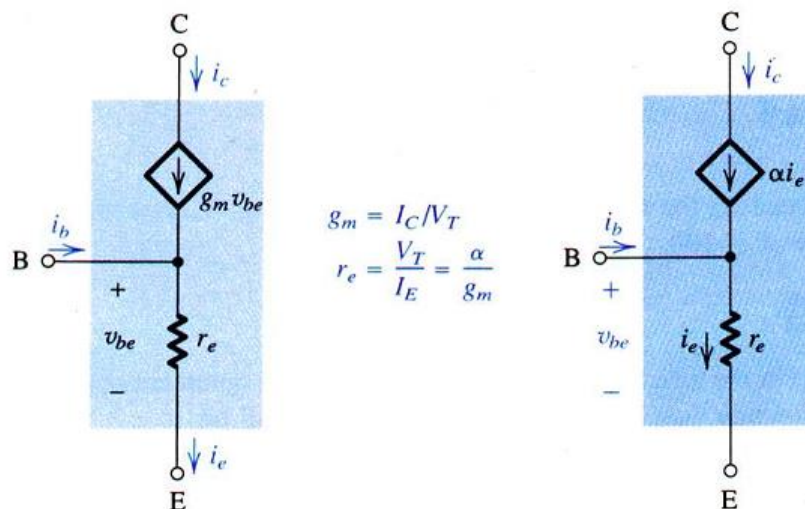
Obs: Neste modelo se V_{CE} varia, $I_C = \text{cte.}$ Prof. Pedro Xavier

Modelos equivalentes para pequenos sinais



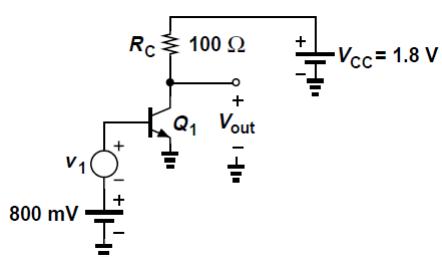
Modelos equivalentes para pequenos sinais

Modelo T



Exercício (Razavi)

- Determine V_{out}



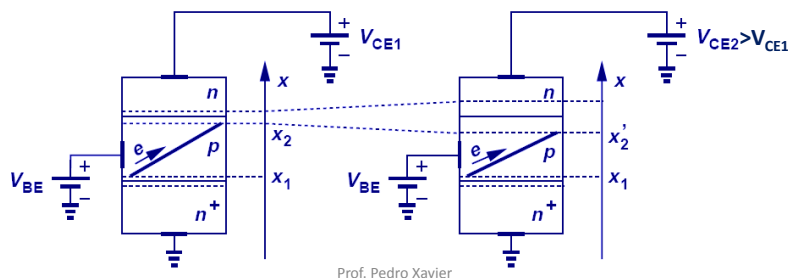
$$v_{1pp} = 1\text{mV}$$

$$I_S = 3 \times 10^{-16}\text{ A}$$

$$\beta = 100$$

Efeito Early – Modulação da Largura de Base

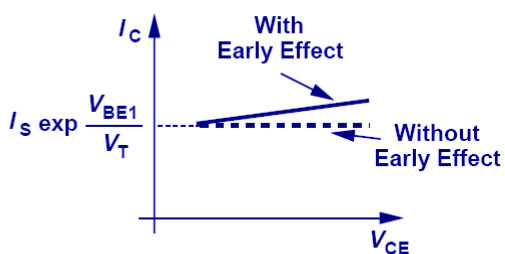
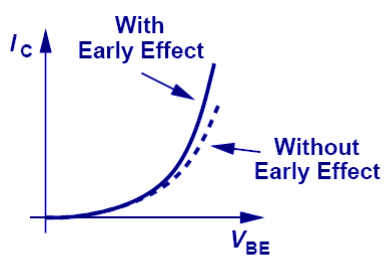
- A largura da junção BC aumenta com V_{BC} e/ou V_{CE} , diminuindo a largura efetiva da base
- O perfil de n_p muda, fica mais inclinado, mudando a corrente de difusão de e^- e I_C .



Efeito Early – Modulação da Largura de Base

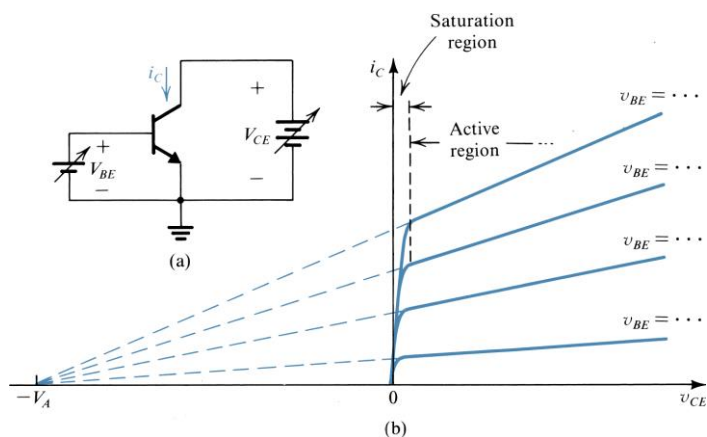
$$I_C = I_S \exp \frac{V_{BE}}{V_T} \left(1 + \frac{V_{CE}}{V_A} \right)$$

Tensão Early

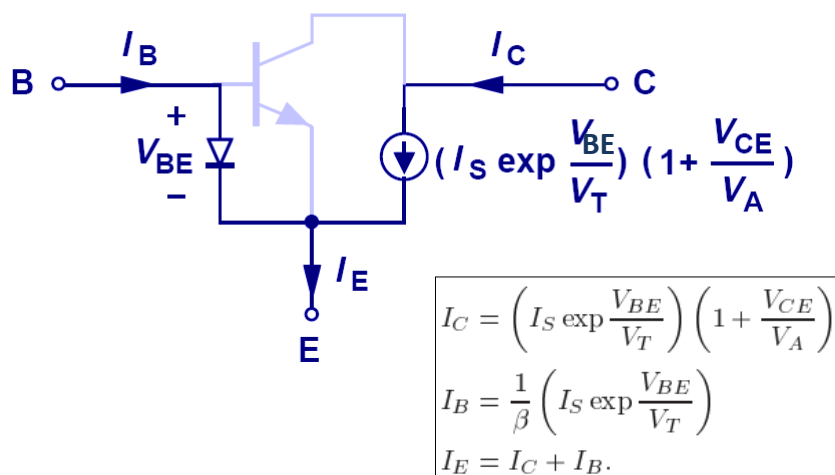


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Efeito Early – Modulação da Largura de Base

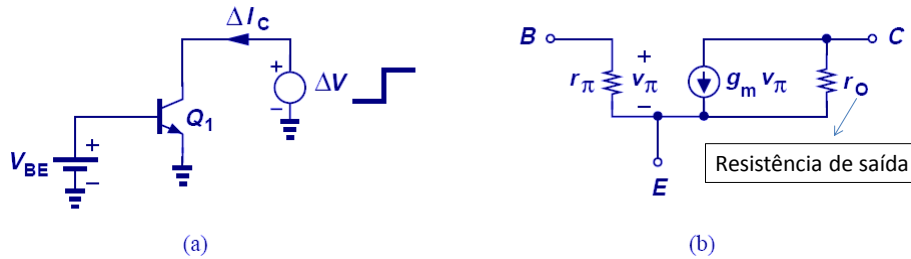


Modelo de grandes sinais (região ativa)



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Modelo de pequenos sinais

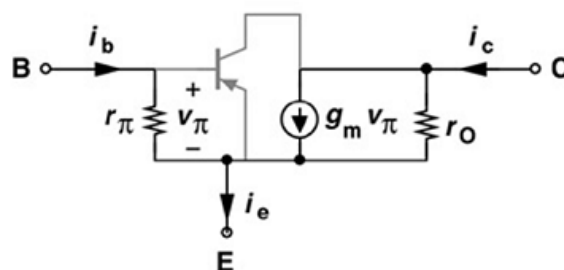


$$I_C + \Delta I_C = \left(I_S \exp \frac{V_{BE}}{V_T} \right) \left(1 + \frac{V_{CE} + \Delta V_{CE}}{V_A} \right) \Rightarrow \Delta I_C = \left(I_S \exp \frac{V_{BE}}{V_T} \right) \frac{\Delta V_{CE}}{V_A}$$

$$r_O = \frac{\Delta V_{CE}}{\Delta I_C} = \frac{V_A}{I_S \exp \frac{V_{BE}}{V_T}} \Rightarrow \boxed{r_O \approx \frac{V_A}{I_C}}$$

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Observe que o modelo de pequenos sinais é o mesmo independente do TBJ ser NPN ou PNP



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Parâmetros do Modelo em Termos das Correntes de Polarização cc :

$$g_m = \frac{I_C}{V_T} \quad r_e = \frac{V_T}{I_E} = \alpha \left(\frac{V_T}{I_C} \right)$$

$$r_\pi = \frac{V_T}{I_B} = \beta \left(\frac{V_T}{I_C} \right) \quad r_o = \frac{V_A}{I_C}$$

Em termos de g_m :

$$r_e = \frac{\alpha}{g_m} \quad r_\pi = \frac{\beta}{g_m}$$

Em termos de r_e :

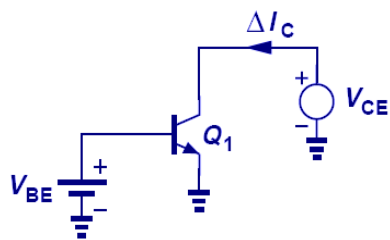
$$g_m = \frac{\alpha}{r_e} \quad r_\pi = (\beta + 1)r_e \quad g_m + \frac{1}{r_\pi} = \frac{1}{r_e}$$

Relações entre α e β :

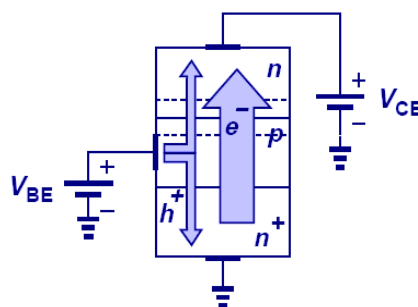
$$\beta = \frac{\alpha}{1 - \alpha} \quad \alpha = \frac{\beta}{\beta + 1} \quad \beta + 1 = \frac{1}{1 - \alpha}$$

Saturação

- As duas junções estão polarizadas diretamente
- $V_{BC} > 0,4$ V: Saturação forte
- $V_{BC} < 0,4$ V: Saturação fraca (despreza a corrente do diodo coletor- base)



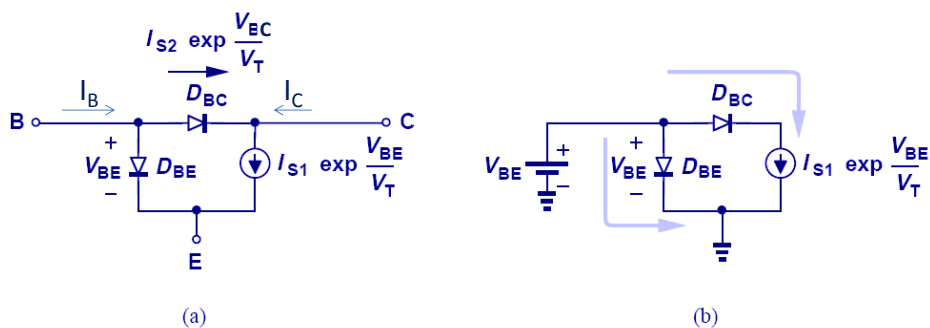
(a)



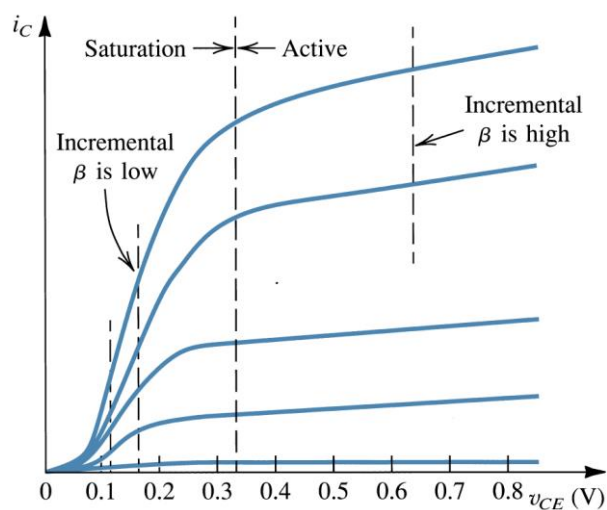
(b)

Saturação

- Para $V_{BC} < 0,4 \rightarrow I_C \cong I_{S1} \exp(V_{BE}/V_T)$
- Para $V_{BC} > 0,4 \rightarrow I_C = I_{S1} \exp(V_{BE}/V_T) - I_{S2} \exp(V_{BC}/V_T)$
- I_B aumenta e I_C diminui $\rightarrow \beta$ diminui



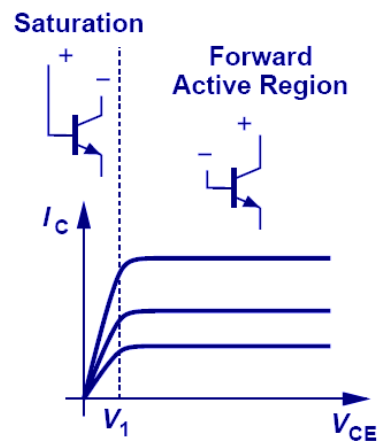
Saturação



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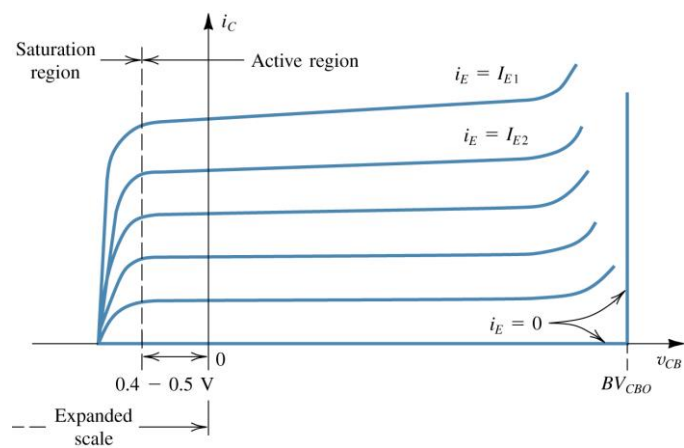
Saturação

- V_{CE} diminui
- Para saturação forte:
 $V_{CEsat} = 200\text{mV}$



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Saturação

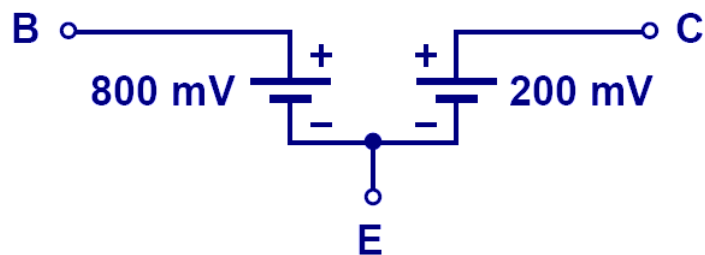


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Saturação

- Modelo para saturação forte:

$$V_{CEsat} = 200\text{mV}$$

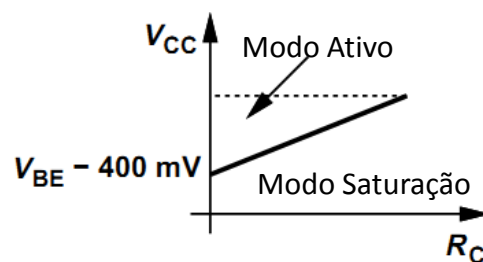
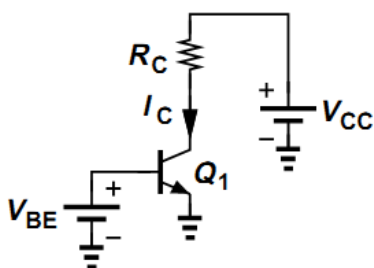


Obs: Menor resposta em frequência.

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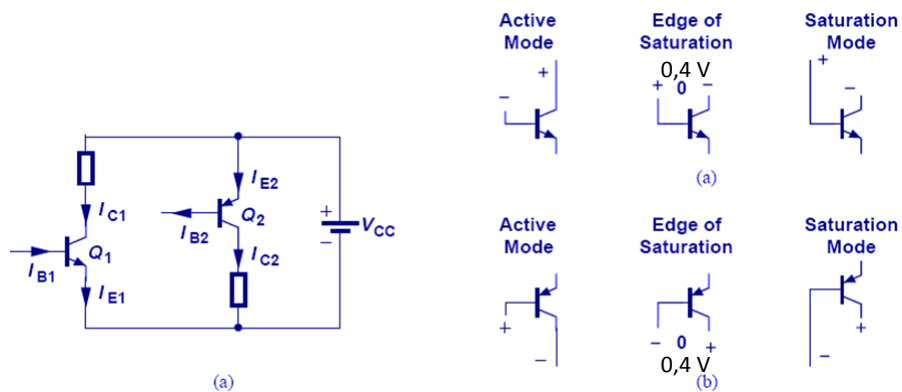
Limite Modo Saturação - Ativo

- Região Ativa: $V_{CC} \geq I_C R_C + (V_{BE} - 400\text{mV})$



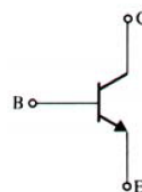
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Resumo



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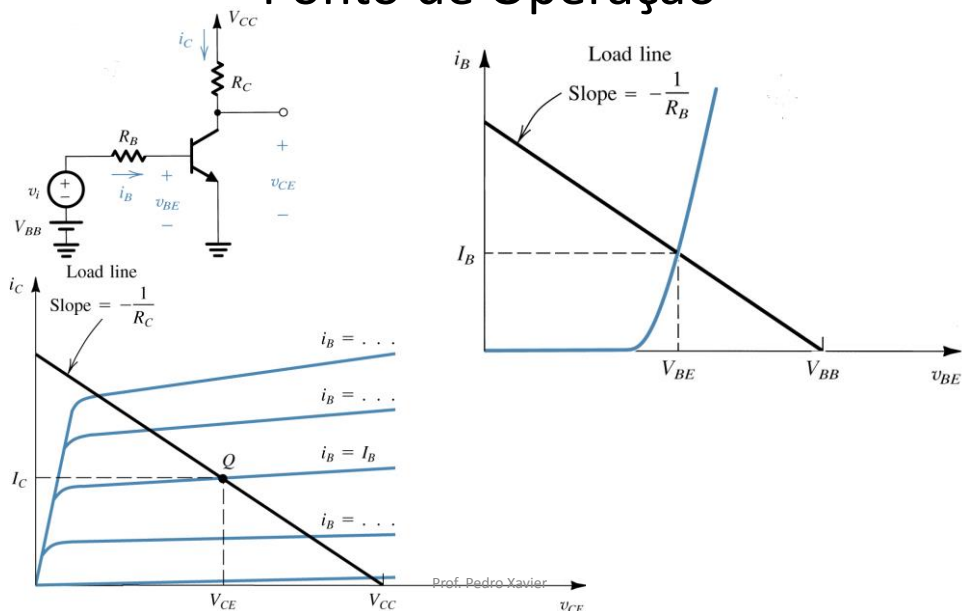
Modos de operação



Modo	JBE	JBC
Corte	Reversa	Reversa
Ativo direto	Direta	Reversa
Saturação	Direta	Direta

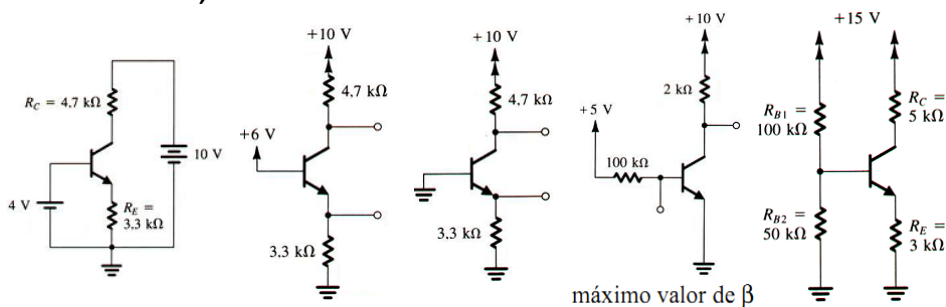
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Ponto de Operação



Análise cc

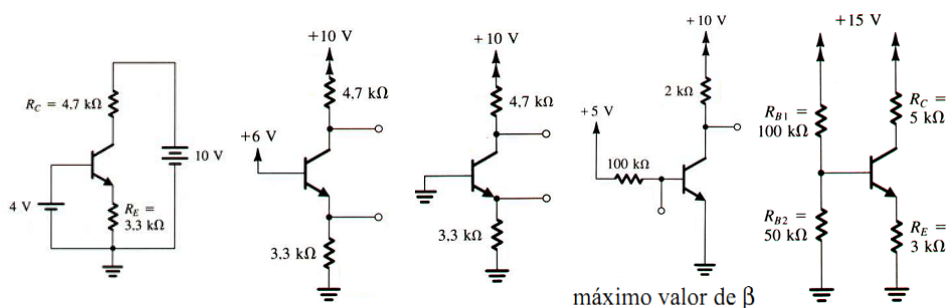
- Determine todas tensões e correntes dos circuitos a seguir ($\beta=100$). Considere $V_{BE}=0,7V$.



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Análise cc

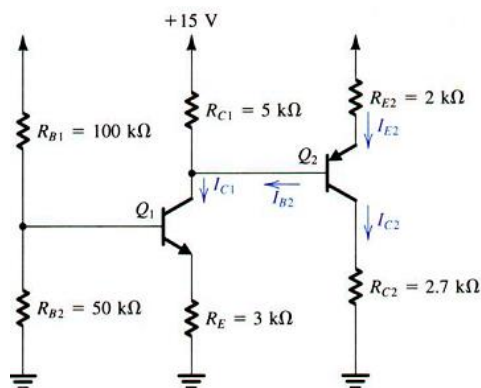
- Determine todas tensões e correntes dos circuitos a seguir ($\beta=100$).



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Análise cc ($V_{BE} = 0,7\text{V}$)

- Determine todas tensões e correntes dos circuitos a seguir ($\beta=100$).



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Fontes de figuras da aula

- Aula do prof. Fabiano Fruett
- Introdução à física dos semicondutores (H.A. Mello)
- Fundamentos da microeletrônica (Razavi)
- Microeletrônica (Sedra)

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Sugestão de estudo

- Sedra/Smith cap. 4 seções 4.5 até 4.8
- Razavi cap. 4 a partir da seção 4.4.3

Para saber mais:

Paul R. Gray e Robert G. Meyer, Analysis and Design of Analog integrated Circuits, John Wiley & Sons