Lesson 5

Digital Control of Three-Phase DC/AC Converters: Current Control Techniques

Digital Hysteresis Control

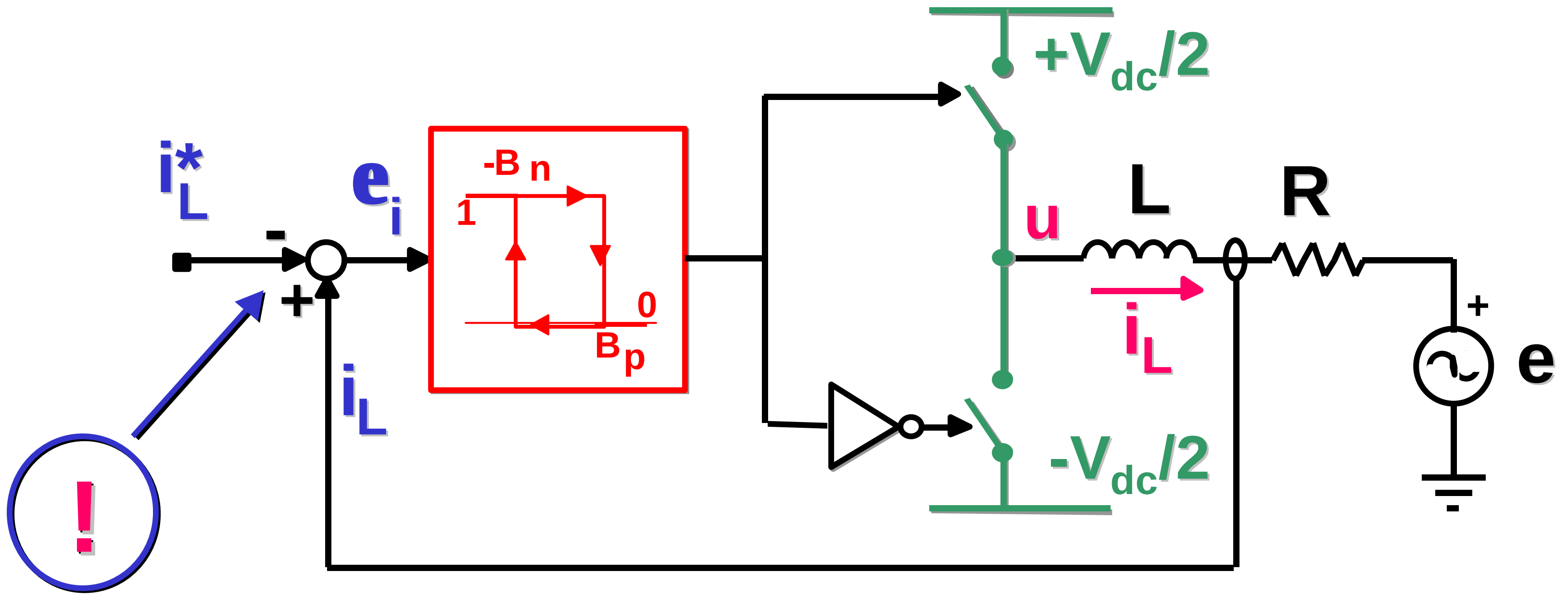
Digital Hysteresis Control

- Thank to its inherent non-linearity, the hysteresis current control is capable of providing the fastest possible dynamic response.
- Using this technique, it is possible to achieve the maximum exploitation of the power converter. The limit to current regulation capability, in fact, is only given by the power converter design.
- The hysteresis current control is inherently stable and robust to load variations or any other type of dynamic perturbations.

Digital Hysteresis Control

- The generation of non-dc current waveforms implies the variation of the instantaneous switching frequency.
- This is not desirable because:
    - the design of converter's output filters is more complicated and less effective;
    - in case of motor drive applications, acoustic noise due to mechanic resonances may be generated.

Digital Hysteresis Control



Single-phase schematic of the hysteresis current control. The hysteresis bands B_p, B_n are supposed to be fixed.

Digital Hysteresis Control

$$u = R \cdot i_L + L \, {di_L}/{dt} + e$$ Load equation

$$e_i = i_L - i_L^*$$ Current error

$$u^* = R \cdot i_L^* + L \, {di_L^*}/{dt} + e$$ Reference voltage

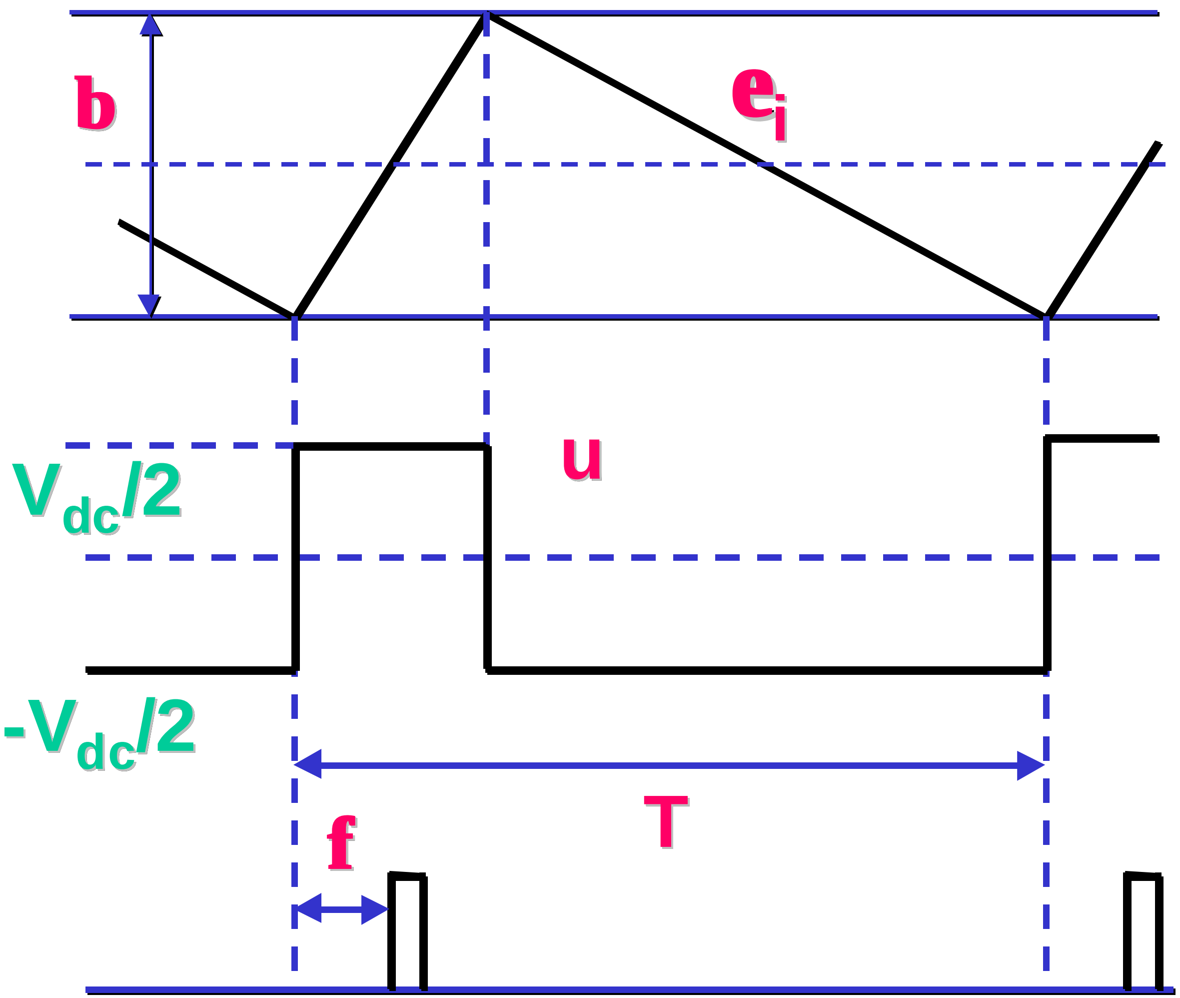
$$u - u^* = R \cdot e_i + L \, {de_i}/{dt}$$ Current error dynamic equation

Digital Hysteresis Control

$$u - u^{*} = R \cdot e_i + L \, de_i / dt$$

- **Normally the resistive term can be neglected and the reference voltage u^{*} can be considered constant during a modulation period.**
- **Therefore, the current error has a triangular shape (right-hand side is constant) and the average of u over a modulation period is equal to u* (total current variation is 0).**

Digital Hysteresis Control



Current error and hysteresis band.

Inverter voltage pulses.

Synchronization clock.

Digital Hysteresis Control

- It is possible to derive the following **'period'** equation:

$$T = \frac{4bL}{V_{dc} \cdot \left(1 - u_n^2\right)}$$

where:

$$u_n = u^* \Big/ \left(V_{dc} \big/ 2 \right)$$

Digital Hysteresis Control

The ‘period’ equation shows that:

- if **b** is constant and u_n varies the period T also varies;
- to get a constant switching frequency ($1/T_d$) the hysteresis band **b** has to be dynamically modified, according to this equation:

$$b = \frac{V_{dc} \cdot T_d}{4 \cdot L} \cdot \left(1 - u_n^2\right)$$

Digital Hysteresis Control

- The application of the hysteresis current control to three phase systems with insulated neutral is made a little more complicated by the unavoidable interference among the phase currents.
- It is anyway possible to strongly reduce the interference by suitably manipulating the current error.
- This only requires a simple additional analog circuit.

Digital Hysteresis Control

- In a three-phase system with insulated neutral the load equation must be modified to take into account the load midpoint voltage (neutral voltage).

$$\underline{u} = R \cdot \underline{i_L} + L \, \frac{d\underline{i_L}}{dt} + \underline{e} + u_o \cdot \underline{1}$$

where u_o is the load midpoint voltage (neutral voltage) and $\underline{1}$ is the unity vector.

$$u_o = \frac{(u_1 + u_2 + u_3)}{3}$$

Digital Hysteresis Control

- With the same definitions and procedure of the single phase case, the following dynamic equation can be derived for the current error:

$$\underline{u} - \underline{u}^{*} - u_o \cdot \underline{1} = R \cdot \underline{e_i} + L \frac{de_i}{dt}$$

- Because of the presence of u_o, the current error in a switching period is not triangular and its slope (on each phase) depends on the state of all phases (through u_o). This phenomenon is known as phase-interference.

Digital Hysteresis Control

- To eliminate the phase interference, which negatively affects the hysteresis control behavior, a decoupling term e''_i can be defined as follows:

$$R \cdot \underline{e''_i} + L \frac{d\underline{e''_i}}{dt} = -u_o \cdot \underline{1}$$

which can be easily implemented by filtering the instantaneous voltage u_o with an analog low pass filter having the same time constant of the load (L/R). Tuning is normally required.

Digital Hysteresis Control

- Re-writing the error dynamic equation as a function of the decoupled current error e'_i:

$$e'_i = \underline{e}_i - \underline{e}''_i$$

it is possible to derive the decoupled error e'_i dynamic equation:

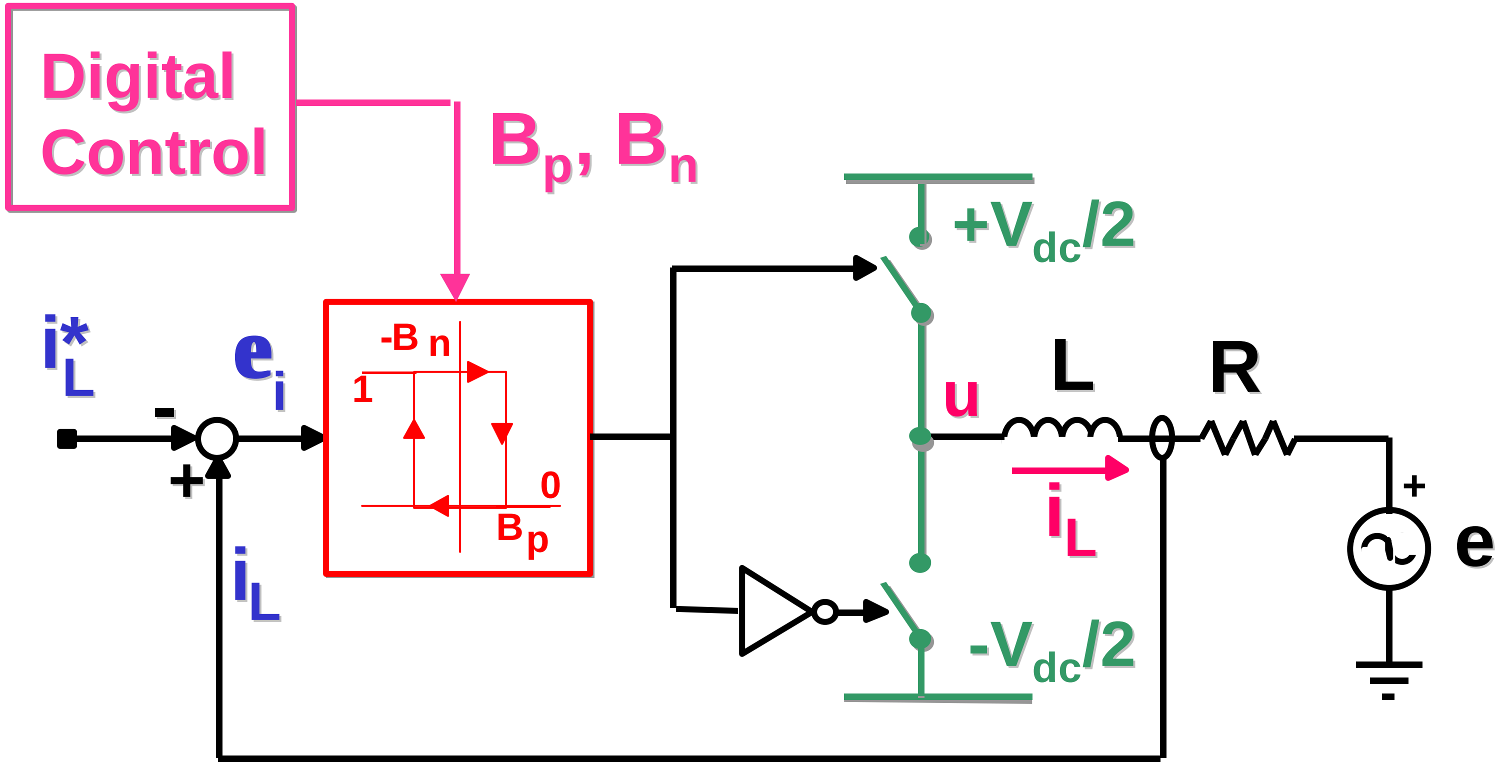
$$\underline{u} - \underline{u}^* = R \cdot \underline{e}'_i + L \, d\underline{e}'_i / dt$$

which no longer depends on the load midpoint voltage u_o.

Digital Hysteresis Control

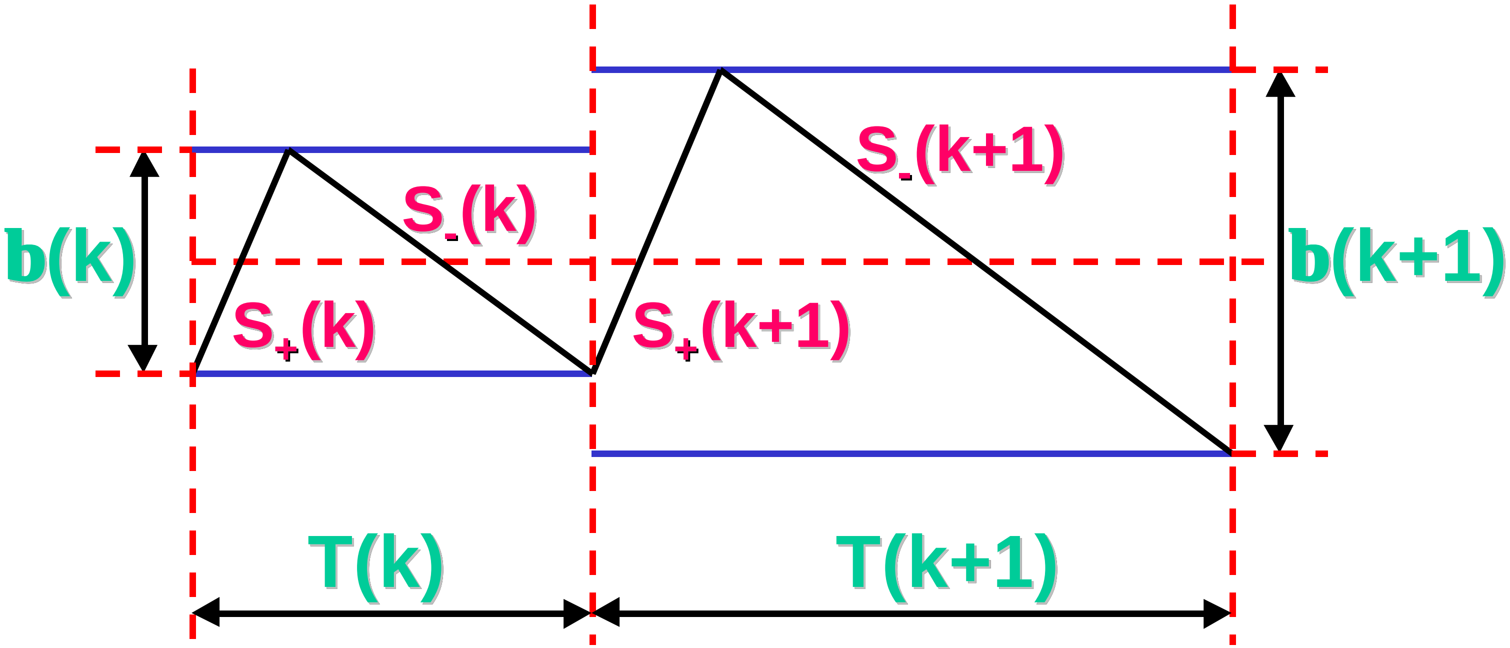
- The structure of the decoupled error dynamic equation is exactly the same of the single-phase case.
- Therefore, once a suitable decoupling circuit is implemented, the three-phase system behaves exactly as three single phase ones, with triangular decoupled current errors, whose slope depends only on the state of the corresponding inverter phase.
- From now on, the explanation of the digital control system for the hysteresis controller will refer to the single phase case.

Digital Hysteresis Control



The controller maintains its analog structure, but a bandwidth digital control is added which ensures constant switching frequency.

Bandwidth Control Algorithm



$\forall$ k:

$$S_+ \cdot T_{on} = S_- \cdot T_{off} = b$$

$$T_{on} + T_{off} = T$$

Bandwidth Control Algorithm

- From the previous equations it is possible to derive:

$$T(k) = \frac{b(k)}{S_{+}(k)} + \frac{b(k)}{S_{-}(k)} = b(k) \times \frac{S_{+}(k) + S_{-}(k)}{S_{p}(k)}$$

and assuming:

$$S_{+}(k+1) = S_{+}(k) \qquad\qquad S_{-}(k+1) = S_{-}(k)$$

we can get:

$$T(k+1) = b(k+1) \times \frac{T(k)}{b(k)}$$

Bandwidth Control Algorithm

- From the previous equations, it is possible to derive the **control equation:**

$$b(k+1) = b(k) \cdot \frac{T_d}{T(k)}$$

where T_d is the **desired switching period.**

- It is worth noting that **this reasoning leads to an algorithm** which is equivalent to a **first order dead-beat control** of the switching period.

Bandwidth Control Algorithm

- The control algorithm is very simple. It only requires time measurements, which can be easily implemented by using the capture function of any micro-controller.
- The algorithm is auto-tuning, does not require any knowledge of the load parameters. They are implicitly estimated by measuring the switching period with a known b.
- The calculation of the 'new' b requires a division. This implies a certain computation time.

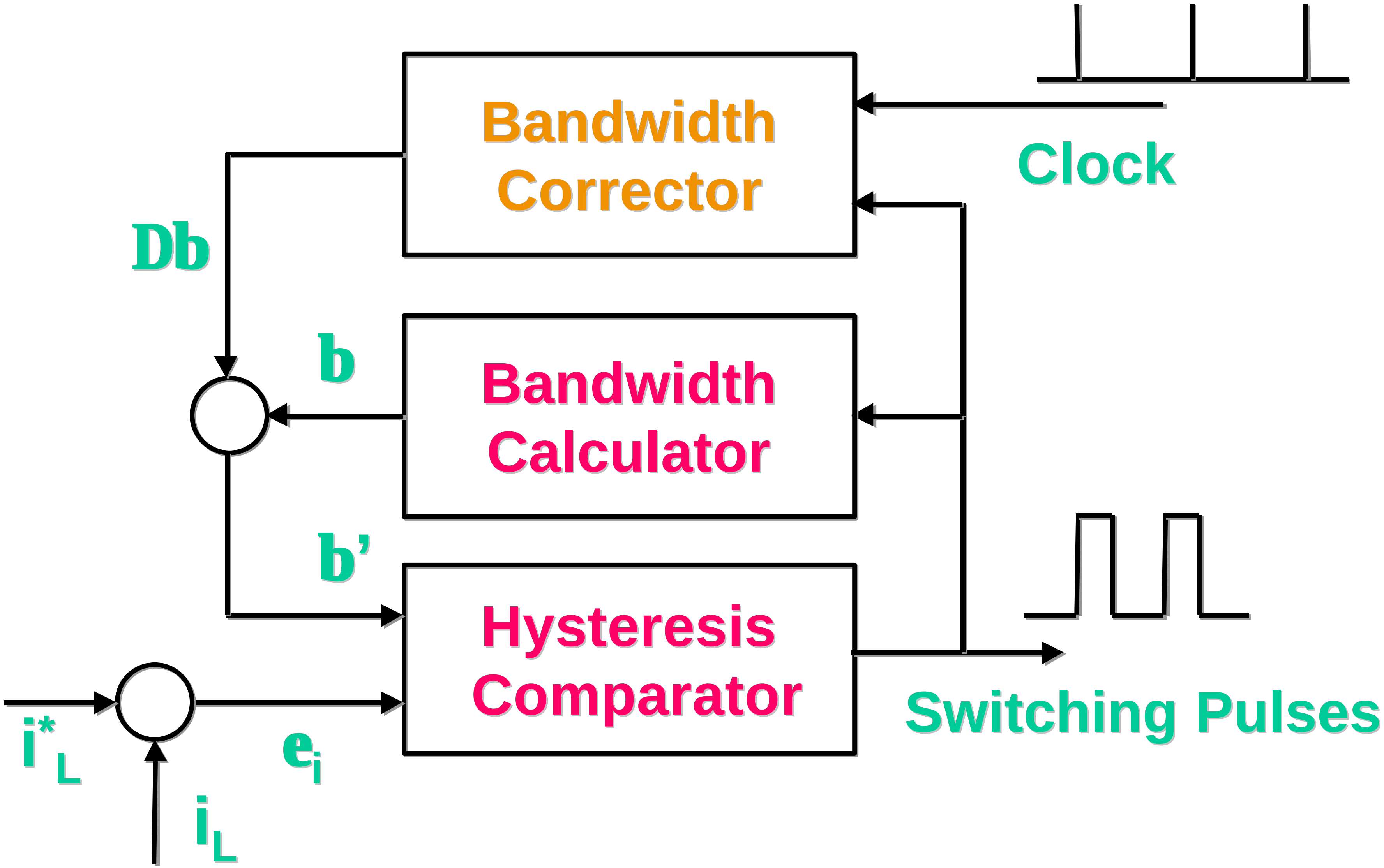
Bandwidth Control Algorithm

- The control algorithm is able to guarantee a good frequency regulation.
- Unfortunately, the switching pulses for the three phases are not phase-controlled. This means that the allocation inside the modulation period of the switching pulses is random.
- This implies a slightly increased current ripple with respect with the optimum pulse allocation (centered pulses).
- Methods to improve the algorithm, including pulses phase control are available.

Bandwidth Control Algorithm

- **A feasible way to regulate the phase shift between the pulses is to lock them to a synchronizing clock.**
- **The time difference between the synchronizing clock and the inverter pulses can be measured and used to modify the bandwidth.**
- **A proper regulator must be designed to stabilize the system.**
- **This solution is equivalent to the implementation of a digital Phase Locked Loop (PLL).**

Bandwidth Control Algorithm



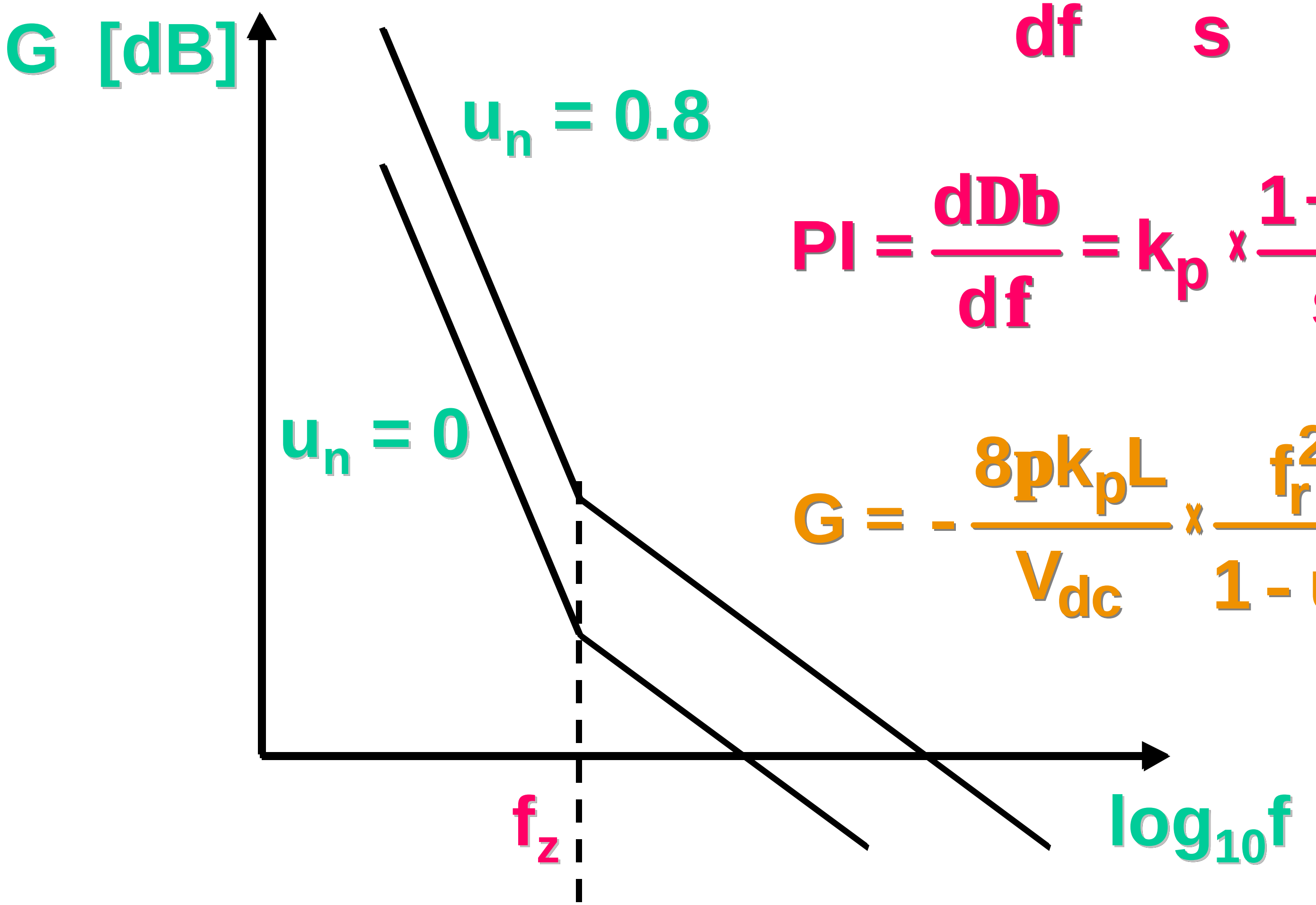
Bandwidth Control Algorithm

- **The design of the bandwidth corrector is normally complicated by the open loop gain variability.**
- **Small signal analysis shows that the hysteresis comparator gain is given by:**

$$HC = \frac{df}{d\beta} = -\frac{V_{dc}}{4 \cdot L \cdot \beta^2} \cdot \left(1 - u_n^2\right) = -\frac{f_d}{\beta}$$

- **This gain, together with the phase-detector (integrator) and the regulator (which is normally a PI) gains gives the open loop gain.**

Bandwidth Control Algorithm



$$PhD = \frac{d\varphi}{df} = \frac{2\pi}{s}$$

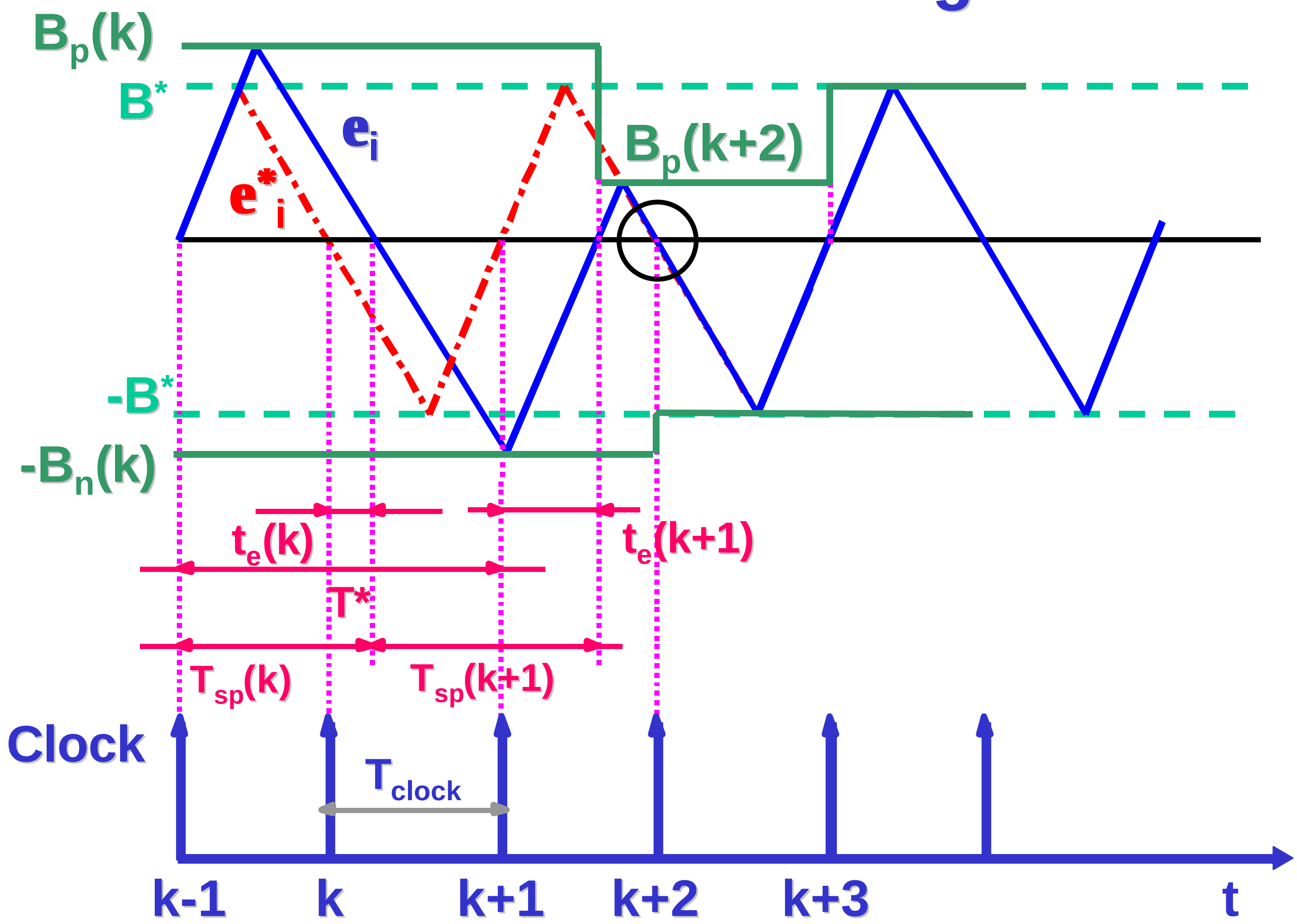
$$PI = \frac{d\Delta\beta}{d\varphi} = k_p \cdot \frac{1 + sT_z}{sT_z}$$

$$G = -\frac{8\pi k_p L}{V_{dc}} \cdot \frac{f_r^2}{1 - u_n^2} \cdot \frac{1 + sT_z}{s^2 T_z}$$

Bandwidth Control Algorithm

- To avoid instability when the modulation index is maximum, the bandwidth of the regulation must be reduced.
- Therefore, the quality of the switching pulses phase regulation is not very high.
- In case of transients, the regulator of the pulse phase induces oscillations, which further decrease the effectiveness of the control.
- Alternative methods to achieve the pulses phase lock can be identified.

Bandwidth Control Algorithm



Bandwidth Control Algorithm

- The algorithm modifies the two hysteresis thresholds independently from each other.
- The input is the timing error $t_e(k)$ between the current error zero crossing and the external synchronization clock.
- At any zero-crossing $t_e(k)$ is measured and the following $t_e(k+1)$ is estimated according to the following equation, where T^* is the desired period ($= 2T_{clk}$):

$$t_e(k+1) = t_e(k) + T_{sp}(k+1) - \frac{T^*}{2}$$

Bandwidth Control Algorithm

- The half period $T_{sp}(k)$ also needs to be estimated according to the following equation:

$$T_{sp}(k+1) = \frac{B_n(k)}{B_p(k)} \cdot T_{sp}(k)$$

- Note that at instant k the thresholds $B_p(k)$ and $B_n(k)$ are known to the algorithm. The algorithm modifies the threshold the current error is not going to. In this case B_p will be modified to get the timing error to zero.

Bandwidth Control Algorithm

- First, **the correct threshold amplitude** must be identified, according to the following equation:

$$B^*(k) = \frac{T^*}{2} \times \frac{B_p(k)}{T_{sp}(k)}$$

- Then, the new value of **threshold $B_p(k+2)$**, which **eliminates the timing error**, can be computed:

$$\frac{B_p(k+2)}{B^*(k)} = \frac{\frac{T^*}{2} - t_e(k+1)}{\frac{T^*}{2}}$$

Bandwidth Control Algorithm

- Substituting all the known quantities in the previous equation the final equation, based on measured data, which updates the threshold and, theoretically, eliminates the error, is obtained:

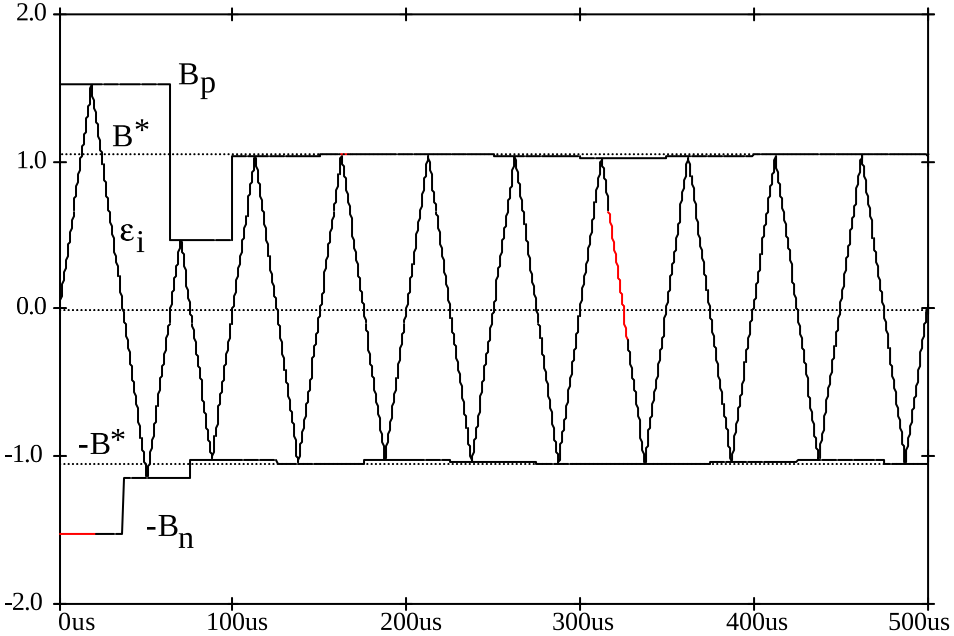
$$B_p(k+2) = B_p(k) \cdot \frac{T^* - t_e(k) - T_{sp}(k) \cdot \dfrac{B_n(k)}{B_p(k)}}{T_{sp}(k)}$$

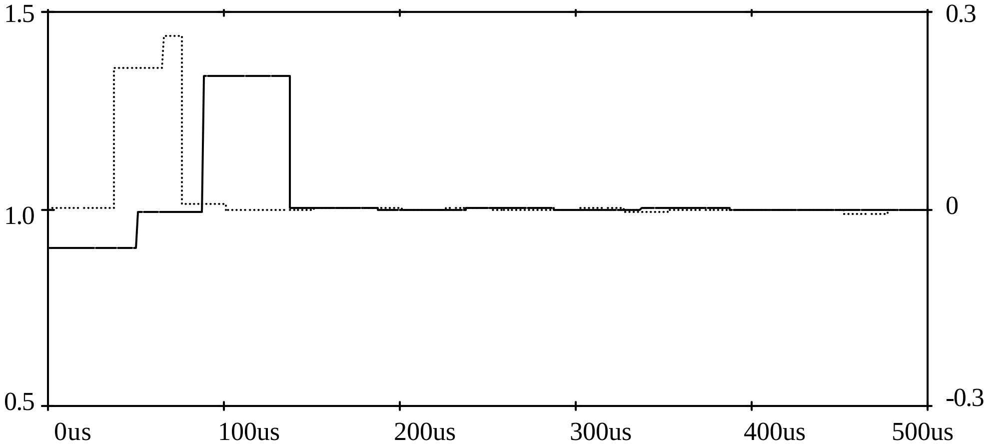
- A totally symmetrical equation can be derived for B_n.

Bandwidth Control Algorithm

- Based on this algorithm a second order dead-beat control of the pulses timing error is achieved.
- In principle, the control eliminates any error in frequency and phase with a modulation period delay (two clock cycles).
- Being the current zero-crossings synchronized with the modulation period, the pulses are automatically centered.
- Dead-times compensation can also be included in the algorithm.

Bandwidth Control Algorithm

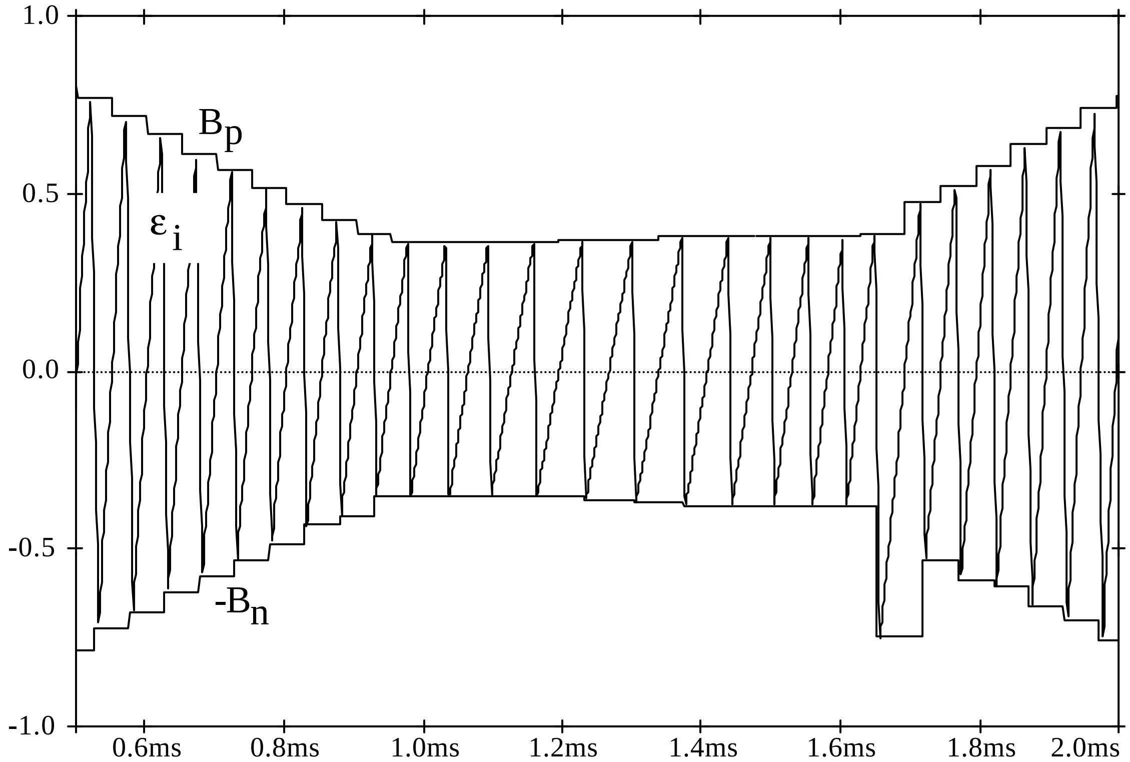




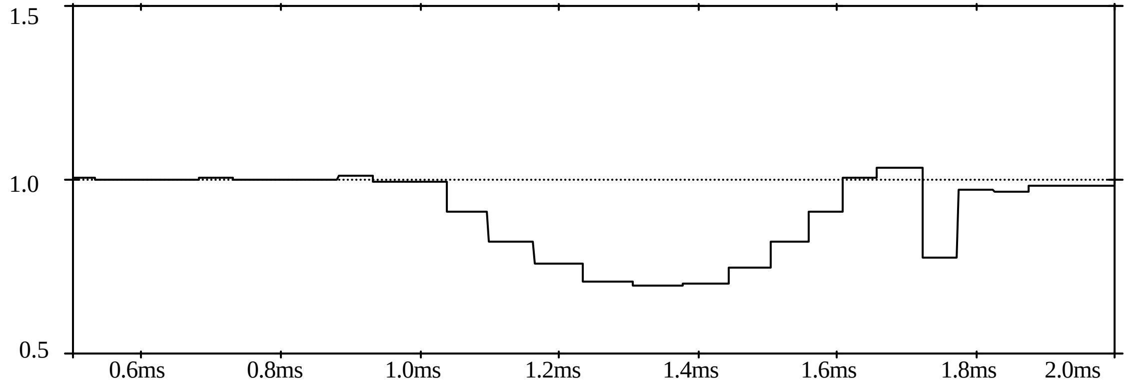
Control's dynamic response to a bandwidth error.

Solid: normalized switching frequency.
Dashed: instantaneous phase error.

Bandwidth Control Algorithm

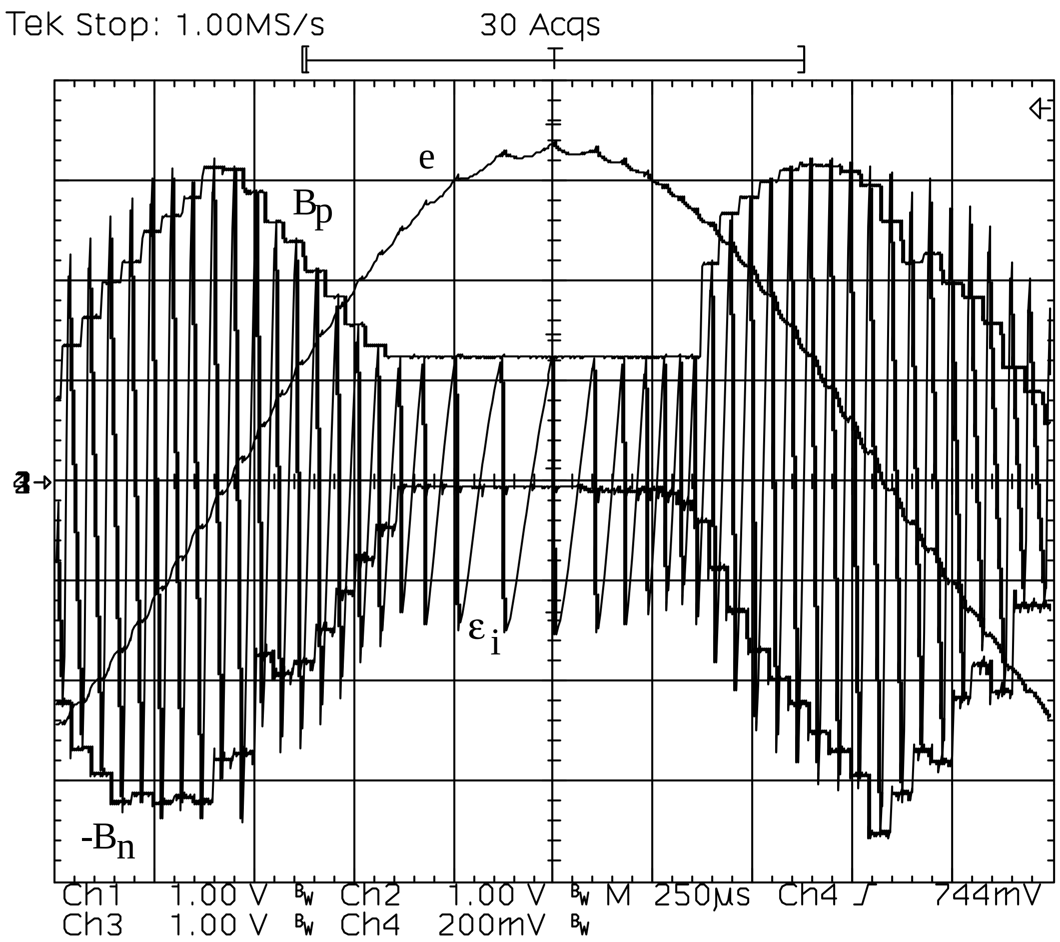


Control operation in saturation mode.



Normalized switching frequency.

Bandwidth Control Algorithm



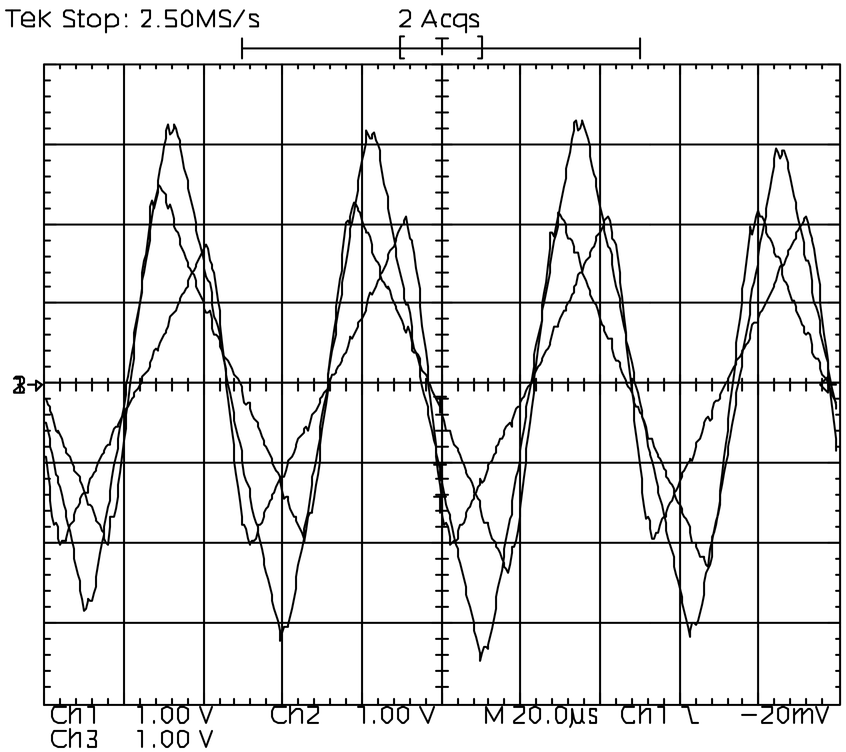
Experimental measurement.
Control operation in saturation mode.

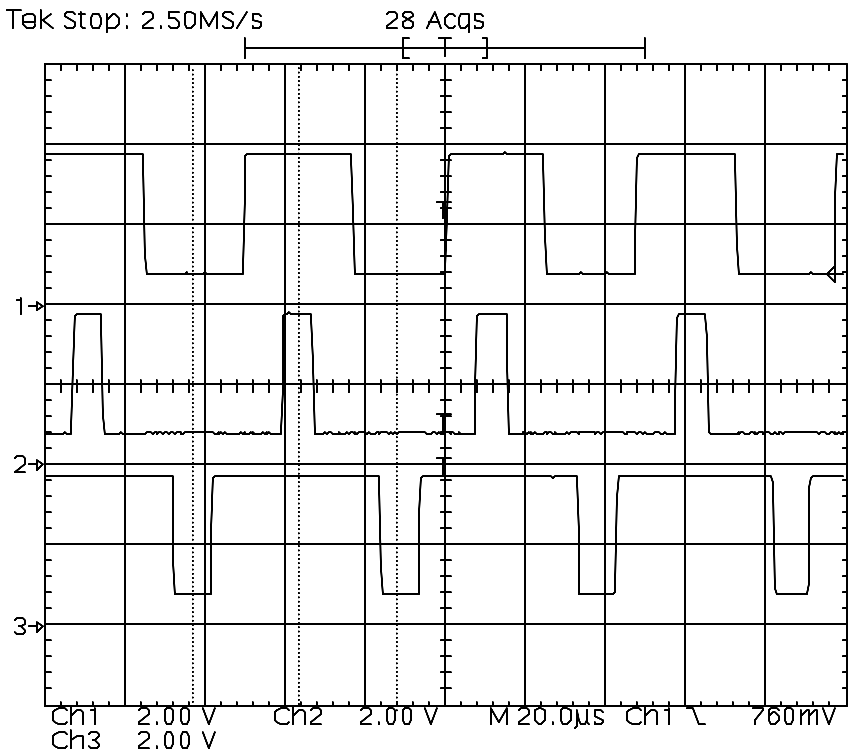
Converter Parameters

DC Link Voltage	300 V
Output Inductor	1.8 mH
Switching Frequency	20 kHz
Nominal Output Power	5 kW

Bandwidth Control Algorithm

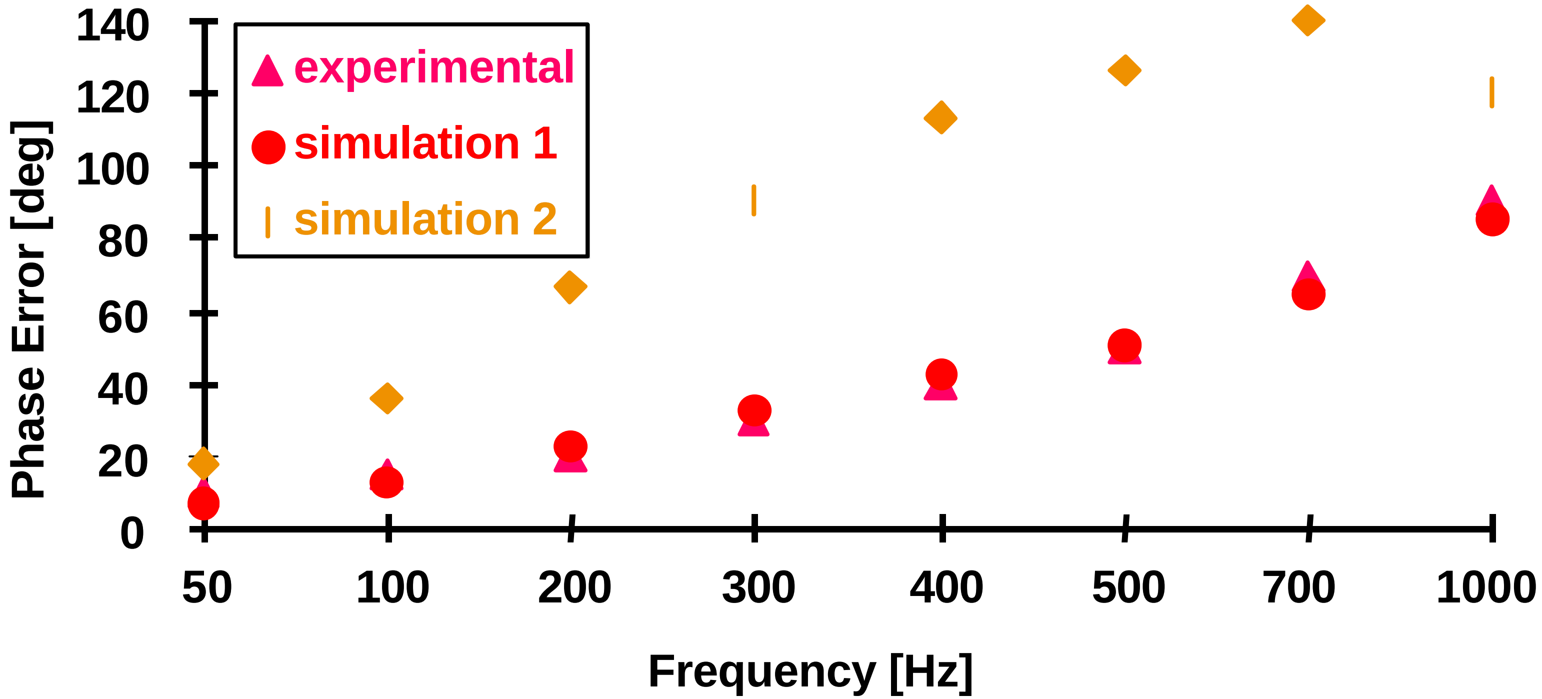
Experimental measurements





Phase current errors **Phase voltage pulses**

Bandwidth Control Algorithm



Phase error in degrees between clock and phase voltage pulses. All plotted data refer to the generation of a sinusoidal current (6 A peak value) with a 0.8 modulation index.

References

[1] L.Malesani and P.Tenti: "A novel **hysteresis control method** for current controlled VSI PWM inverters **with constant modulation frequency"** IEEE Trans. on Industry Applications, Vol.26, No.1, Jan./Feb. 1990, pp.88-92.

[2] Q.Yao and D.G.Holmes: "A simple, novel method for **variable-hysteresis-band current control** of a three phase inverter with constant switching frequency". IEEE IAS'93 Ann. Meet. Conf. Rec., Toronto, Oct. 1993, pp. 1122-1129.

[3] L. Malesani, L. Rossetto, P. Tomasin, A. Zuccato: "**Digital Adaptive Hysteresis Current Control** with Clocked Commutations and Wide Operating Range", IEEE Trans. on Industry Applications, Vol. 32, No. 2, March/April 1996, pp. 316-325.

[4] L.Malesani, P.Mattavelli, S.Fasolo, S.Buso: **"A Dead-Beat Adaptive Hysteresis Current Control",** IEEE IAS'99 Ann. Meet. Conf. Rec., Phoenix, Oct. 1999, pp. 72-79.