Converter topologies for power distribution in the SLHC trackers

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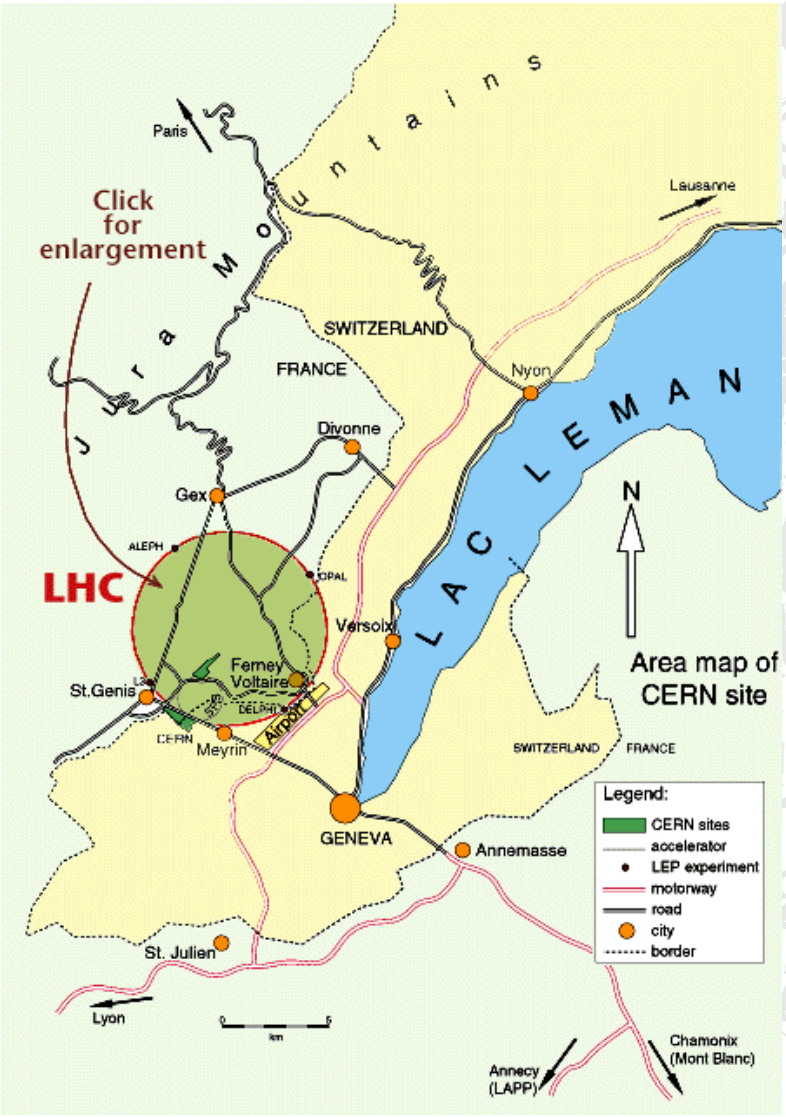
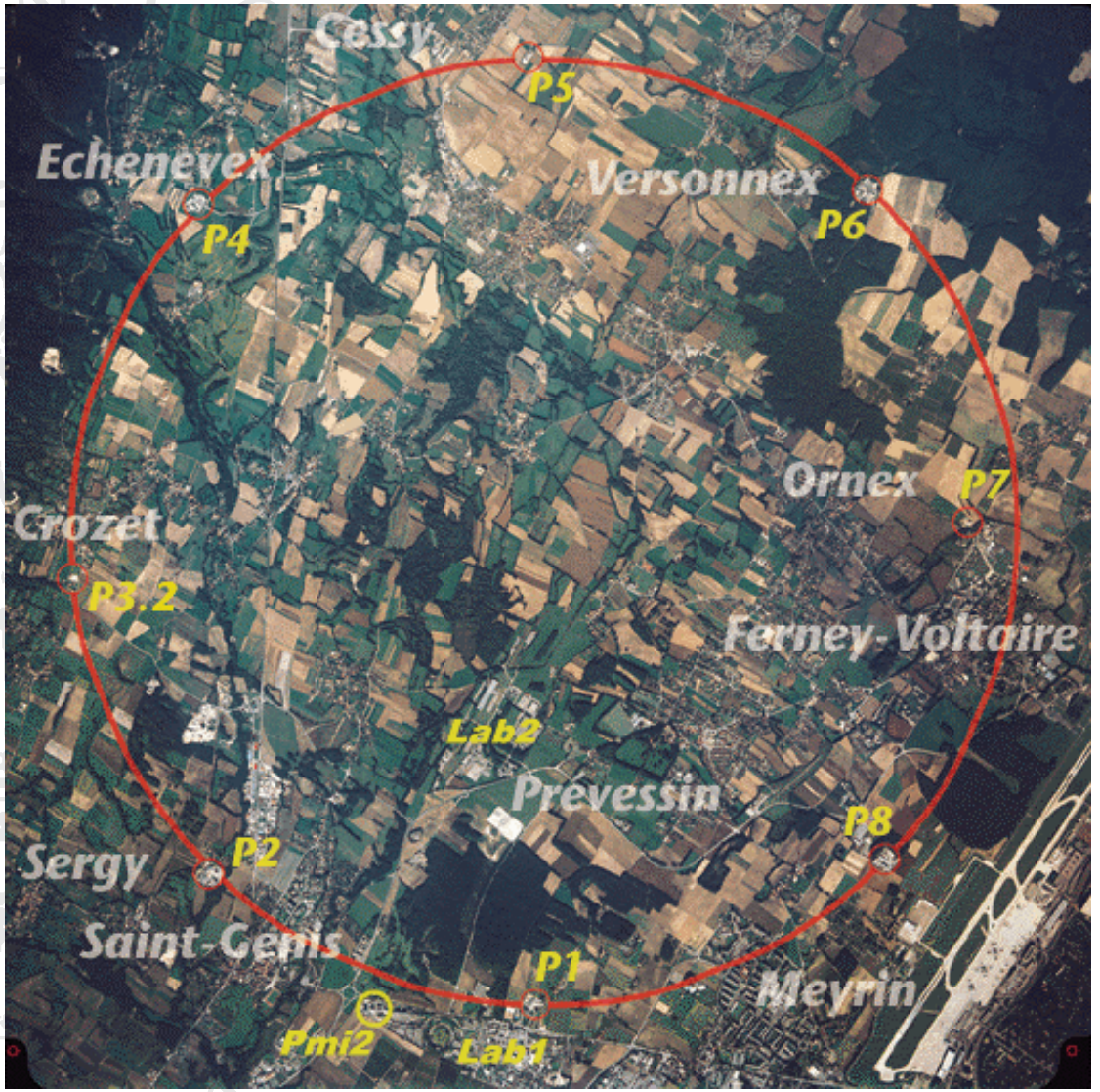
Summary

- Introduction
- Motivation
- Design constraints
- Circuit topologies for POL converters
- Two phase buck with integral voltage divider
- Switched capacitor topologies
- Conclusions

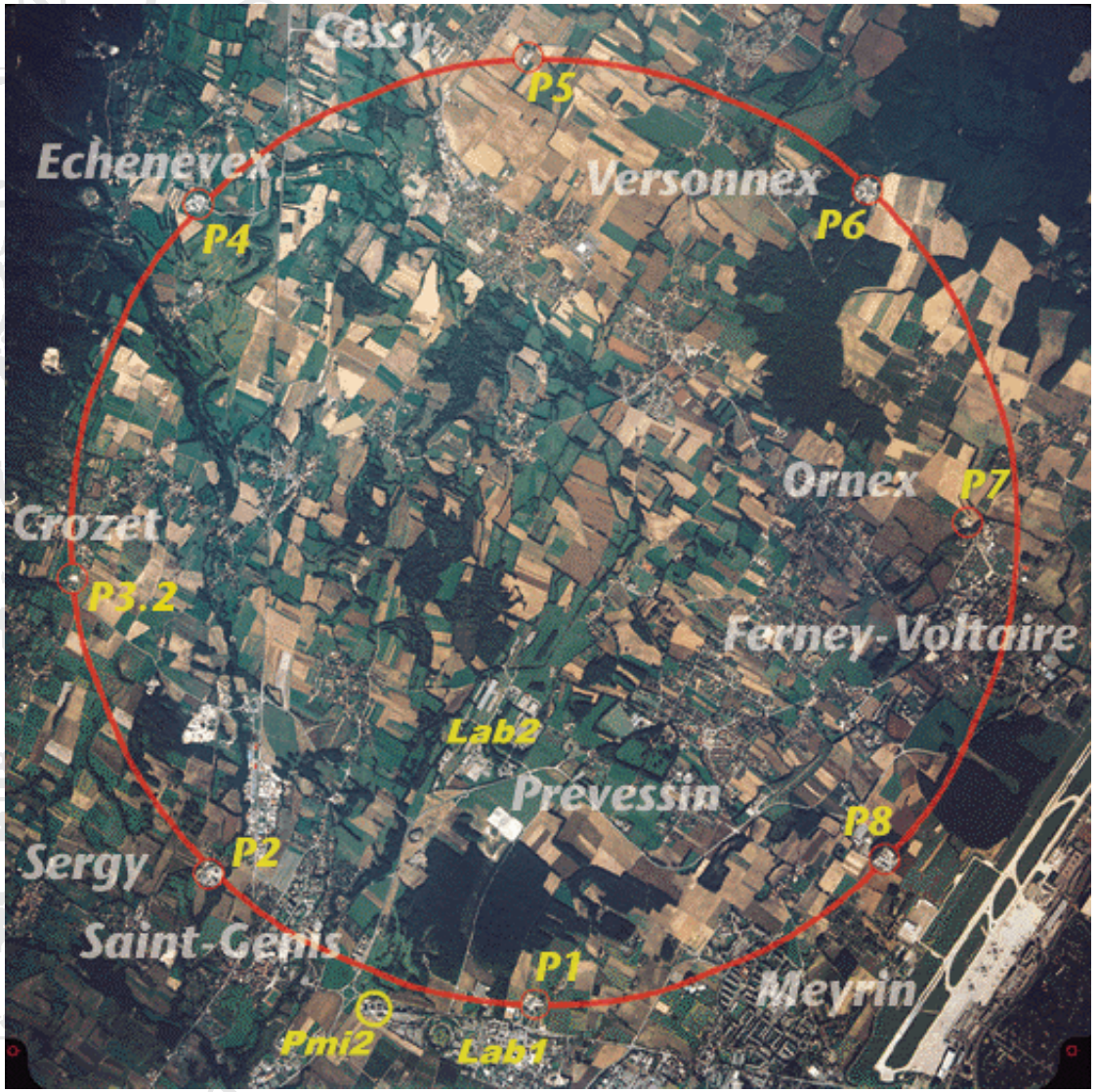
The Large Hadron Collider - LHC



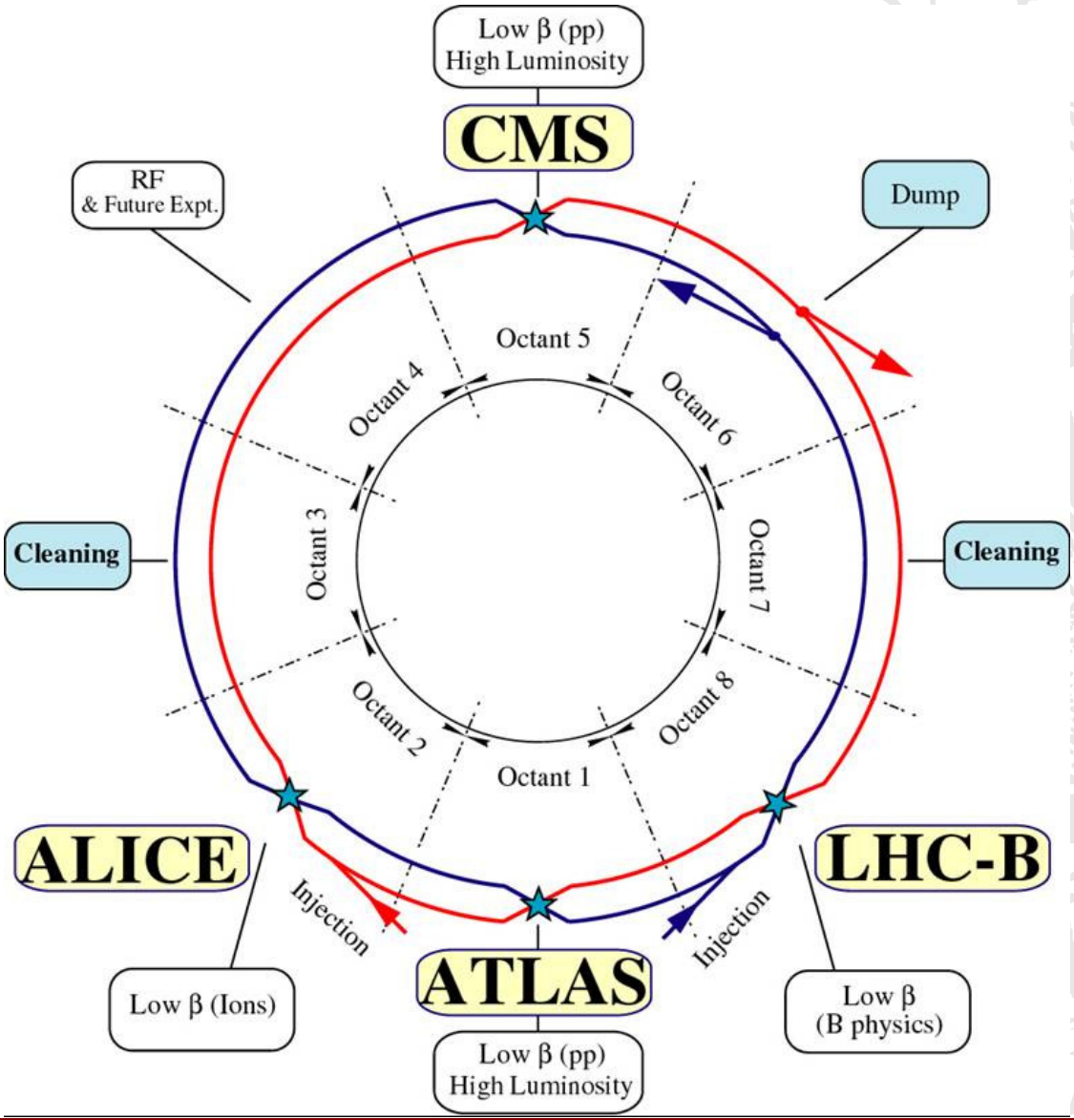


The Large Hadron Collider - LHC

The Large Hadron Collider (LHC) is located inside a circular tunnel, 27 km in circumference. The tunnel is buried around 50 to 175 m underground. It crosses the Swiss and French borders on the outskirts of Geneva.



The Large Hadron Collider - LHC



Four experiments are currently using the LHC infrastructure.

The largest ones are ATLAS and CMS, both dedicated to the study of high energy (up to 14 TeV) collisions of *protons* (quest of the Higgs boson ...).

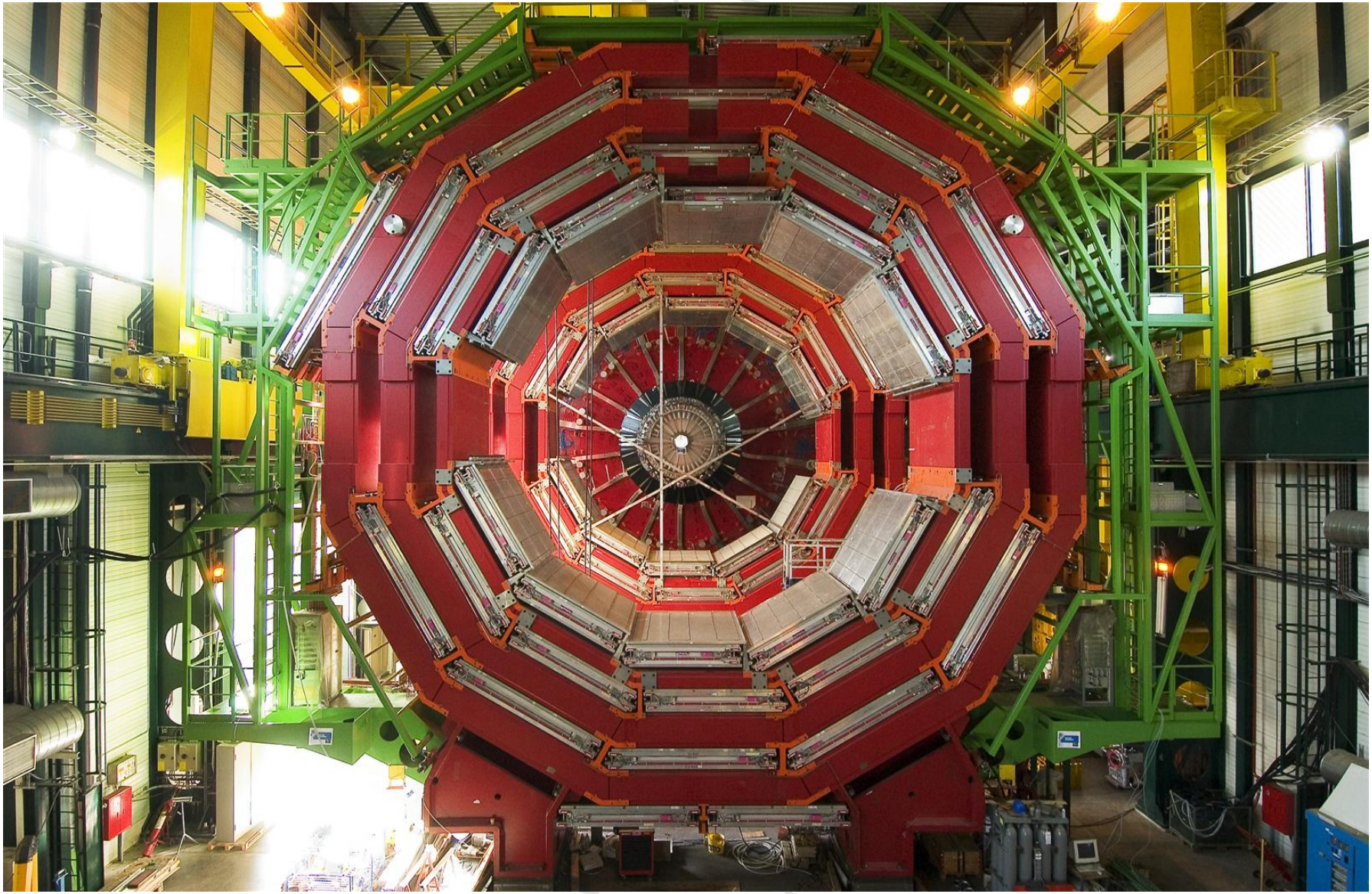
The Large Hadron Collider - LHC

Modern High Energy Physics experiments consist of huge detectors that have to be built with minimum amounts of non-sensitive material, so as to maximize the coverage of sensors and to minimize the unwanted interaction between insensitive infrastructural materials and the particles.

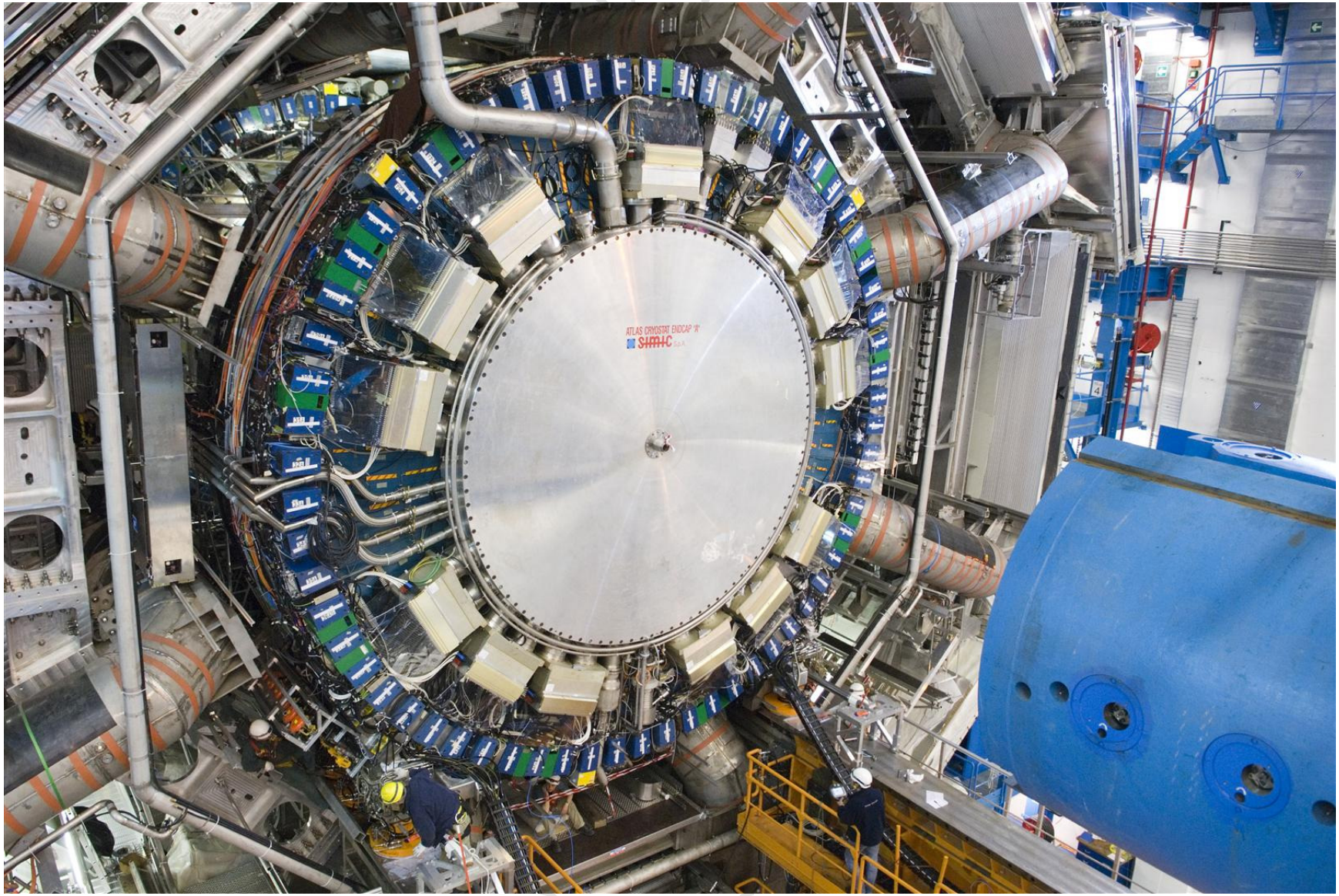
A detector such as the CMS experiment tracker consists of 10 cylindrical layers of thin (3-500 μm) semiconductor sensors, but also of several tons of copper and other metals to bring power to the electronics and consequently to cool it.

The presence of this material is structurally essential, but degrades the precision of the particle position measurement through various phenomena, such as multiple scattering and nuclear interactions.

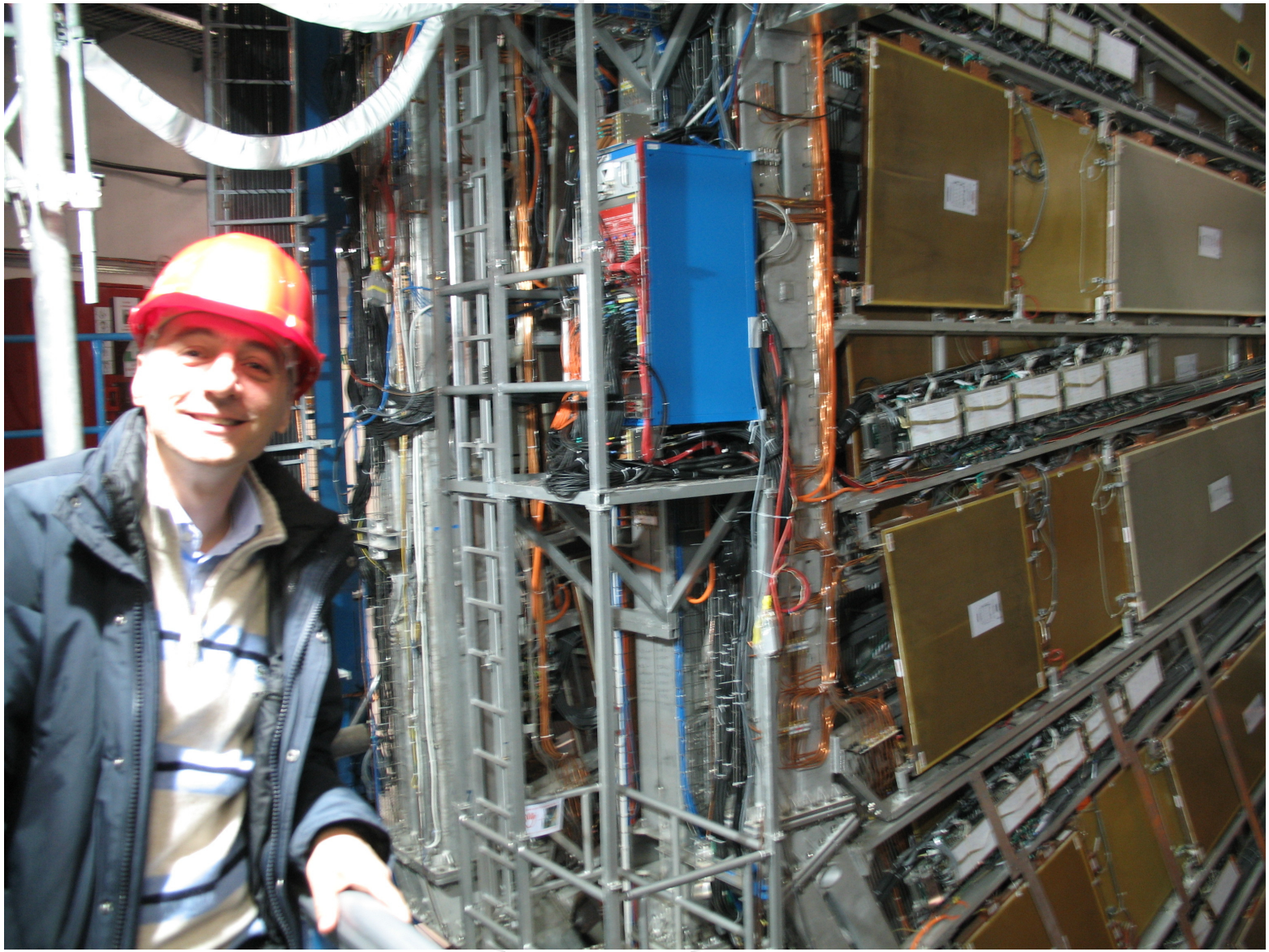
The Large Hadron Collider - LHC



The Large Hadron Collider - LHC



The Large Hadron Collider - LHC



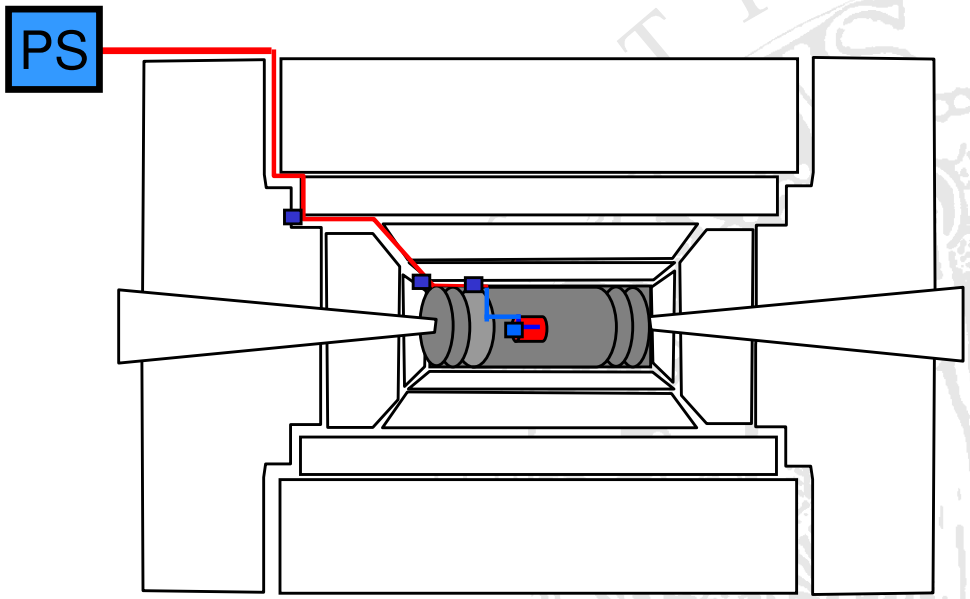
Motivation

The planned increase in the sensitivity of the instrumentation employed in the Large Hadron Collider (LHC) experiments at CERN, calls for a thorough re-design of the power distribution network's architecture.

The powering scheme implemented in the LHC, based on the individual powering of every front-end module from remote power supplies, cannot be applied in the future super LHC because of its inefficiency and of the extra cabling and cooling material that would be required.

One of the considered alternatives involves the development of a distributed power supply network, where integrated point of load converters are to be deployed *inside the trackers,* in a highly hostile environment.

Design constraints



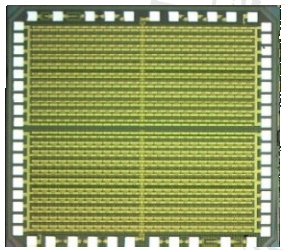
Cross section of ATLAS

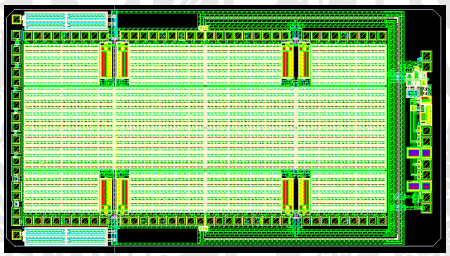
- The converters will be placed **inside the tracker,** therefore they will be exposed to
  - **radiation (> 250Mrad** total dose)
  - **magnetic fields** (2T - **4T)**
- Commercial converters cannot survive because they are not radiation tolerant and use ferromagnetic materials, that saturate at this external magnetic field level.
- It is therefore necessary to develop custom converters, based on ASICs, that meet the HEP requirements

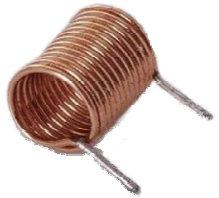
Design constraints

- **Radiation tolerance**

  The specifications require the use of a technology capable to sustain up to 15-20 V (at least). Commercial high voltage technologies are typically conceived for automotive applications. Some of them can be made radiation tolerant by design.





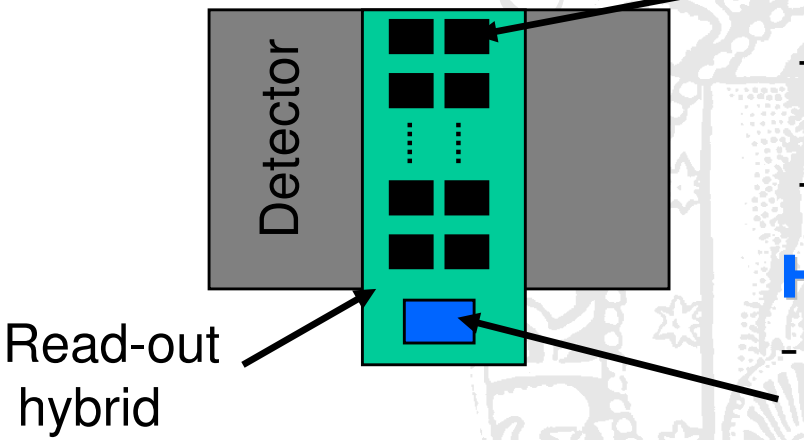


- **Magnetic field tolerance**

  We are compelled to use coreless (air-core) inductors because all the ferromagnetic materials are not usable with an external magnetic field of 2-4 T. This implies the use of very high switching frequencies (> 1 MHz).

Power Distribution in the sLHC

Detector module



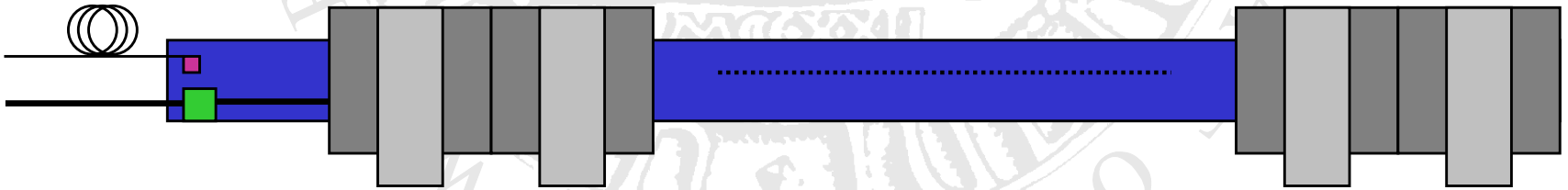
Front-End readout ASIC

- $I_{digital} \geq I_{analog}$ (current projection for ATLAS Short Strip readout is I_{analog} ~ 20mA, $I_{digital}$ ~ 60-100mA)
- 2 power domains: V_{an}=**1.25V**, V_{dig}=**0.9-0.8V** (as low as possible)
- Clock gating might be used => switching load

Hybrid/Module controller

- Ensures communication (data, timing, trigger, possibly DCS)
- Digital functions only
- It might require I/Os at **2.5V**

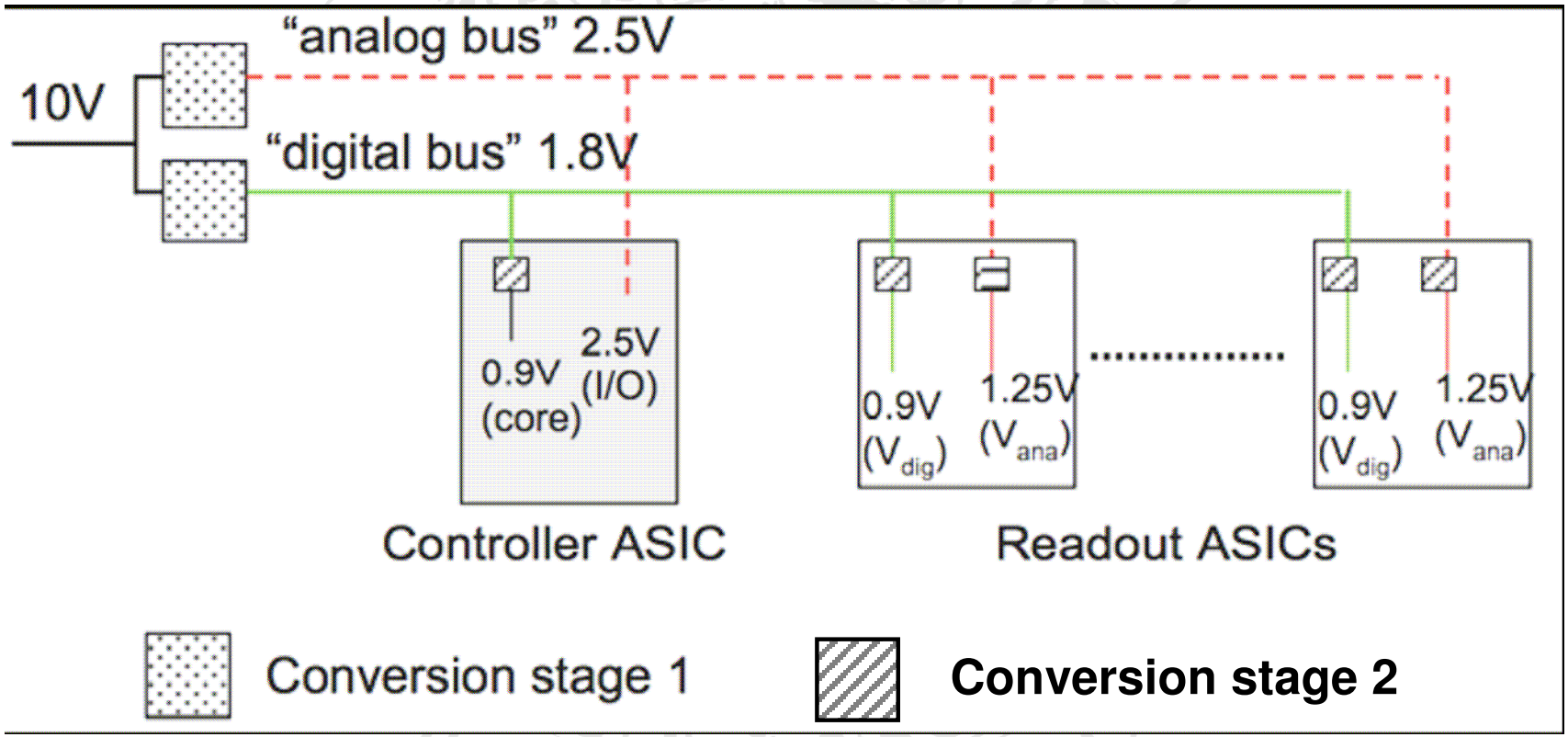
Rod/stave



Other than the **rod/stave controller**, **optoelectronics components** will also have to be used, requiring an additional power domain (2.5-3V)

Power Distribution in the sLHC

Detector module



Power Distribution in the sLHC

Our design options

High frequency commutated (> 1MHz), minimum inductance (air core) buck converters (for conversion stage 1).

Switched capacitor (SC) converters (for conversion stage 2, placed *inside* the ASIC chips).

RAD-HARD Switch Technology

Phase 1 **of the research is the identification of a suitable CMOS technology, allowing the design of both low voltage logic and high voltage (up to 20V) vertical or LD MOS.**

Technology	Technology node	Transistor type	Max Vds [V]	Max Vgs [V]	Before Irradiation R_{on} $[k\Omega \cdot \mu m]$	Displacement Damage R_{on} @ $5 \cdot 10^{15} p^+/cm^2$ $[k\Omega \cdot \mu m]$	Total Ionizing Dose R_{on} @ 100 Mrad $[k\Omega \cdot \mu m]$
A	$0.35\mu m$	Vertical N	80	3.3	16.9	> 1000	17
		LDMOS N	14	3.3	7.1	10.5	7.5
		LDMOS P	80	3.3	41.3	66.4	50
B	$0.25\mu m$	LDMOS N	22	2.5	4.1	6.5	4.8
		LDMOS P	16	2.5	12.2	21.1	15.3
C	$0.18\mu m$	LDMOS N	20	5.5	4.1	14.7	4.7
		LDMOS P			11.2	140.9	47.7
D	$0.18\mu m$	LDMOS N	20	1.8	11.4	992	14
		LDMOS P			26	298	33
		LDMOS N	50	1.8	23.5	> 1000	N.A.
		LDMOS P			40.1	446	N.A.
		LDMOS N	25	5	13.1	N.A.	20
		LDMOS P			25.5	N.A.	39
E	$0.13\mu m$	LDMOS N	20	4.5	7.1	49.6	10.7
		LDMOS P			17.4	177.2	28.7

RAD-HARD Switch Technology

Displacement damage **is due to the impact of neutrons with the crystal lattice. It implies the creation of recombination centers, decreasing the number of available minority carriers. In CMOS processes, this effect is negligible (majority carrier devices) up to very high particle flux levels.**

Total Ionizing Dose **(TID) effects are related to the long term deterioration of the crystal lattice and, in CMOS devices, imply threshold voltage shift and leakage current amplification. Both can be compensated, to a certain extent, by suitable design rules (hardness by design).**

Topologies for POL converters

Phase 2 **of the research is the identification of suitable converter topologies to perform the function of Point of Load (POL) voltage regulators.**

From the devised power distribution architecture we see that step-down (buck) converters are required.

The minimization of inductor size and value, together with the need for minimum ripple call for high frequency (> 1 MHz) operation and, possibly, multi phase arrangements (interleaving).

Topologies for POL converters

Point of Load Converter Specifications

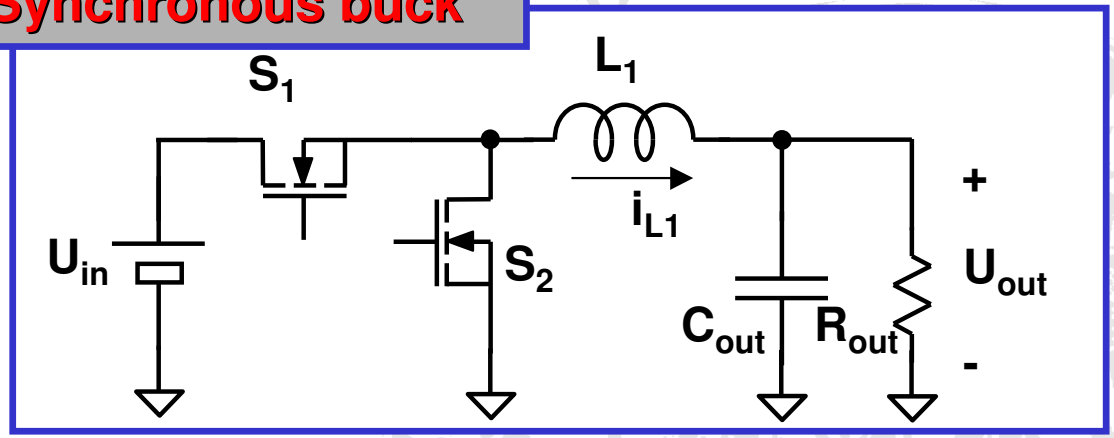
Input voltage, U_{in}	12 V
Output voltage, U_{out}	2.5 V
Output power, P_{out}	7.5 W

Power Switch Specifications

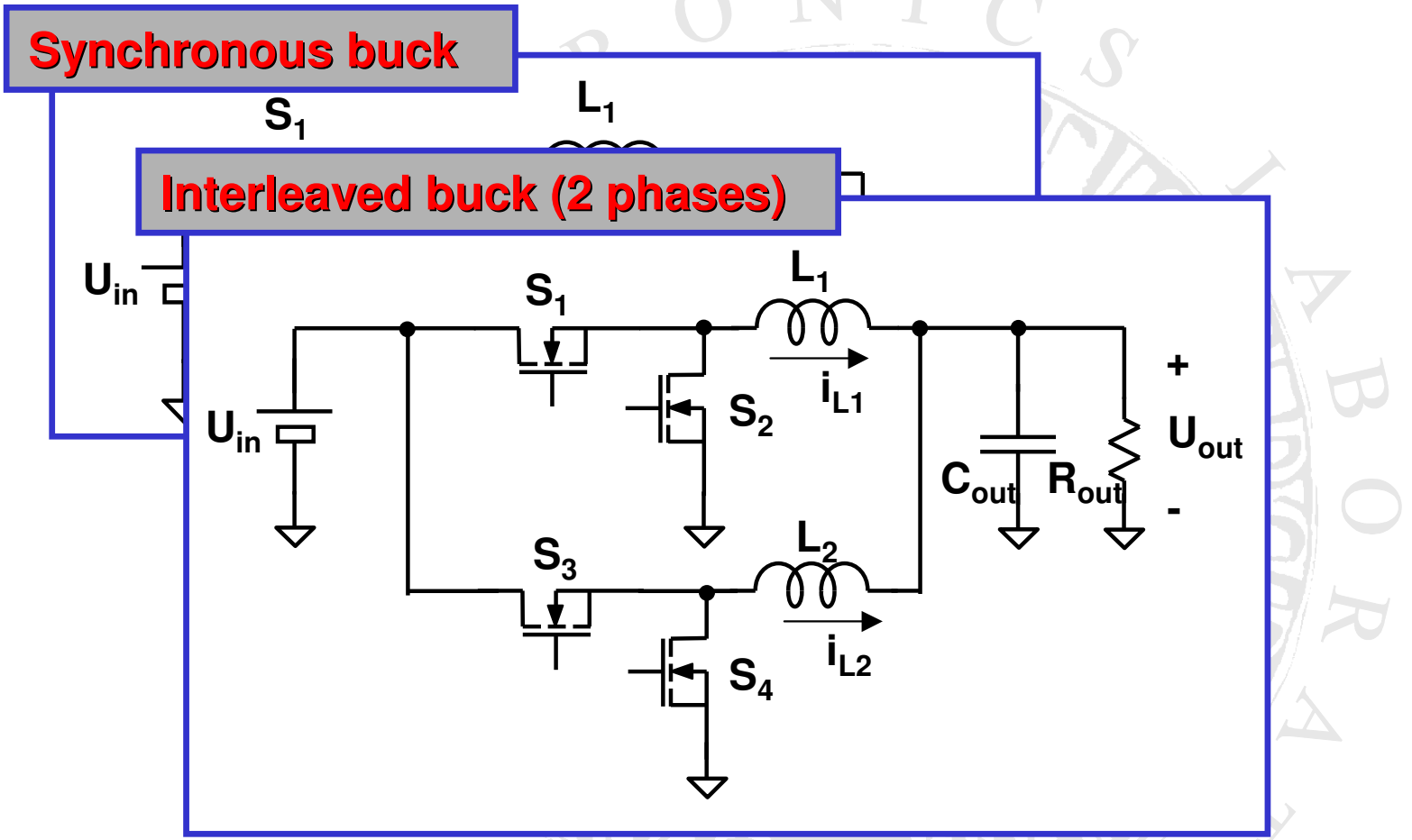
Maximum drain to source voltage	20 V
Maximum RMS current	3 A
Typical on-state resistance @ 25°C	160 mΩ
Typical input capacitance	2000 pF

Topologies for POL converters

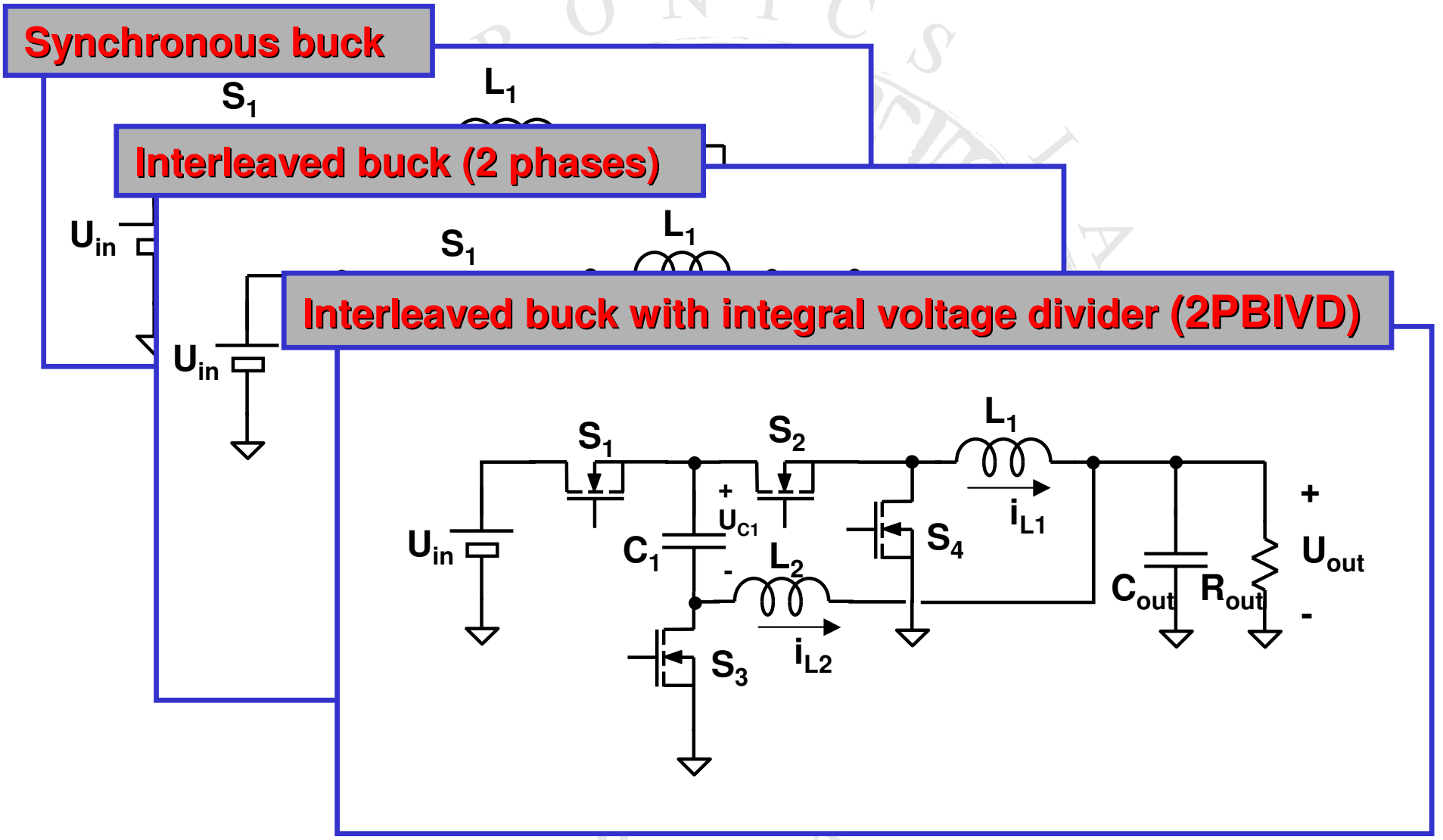
Synchronous buck



Topologies for POL converters



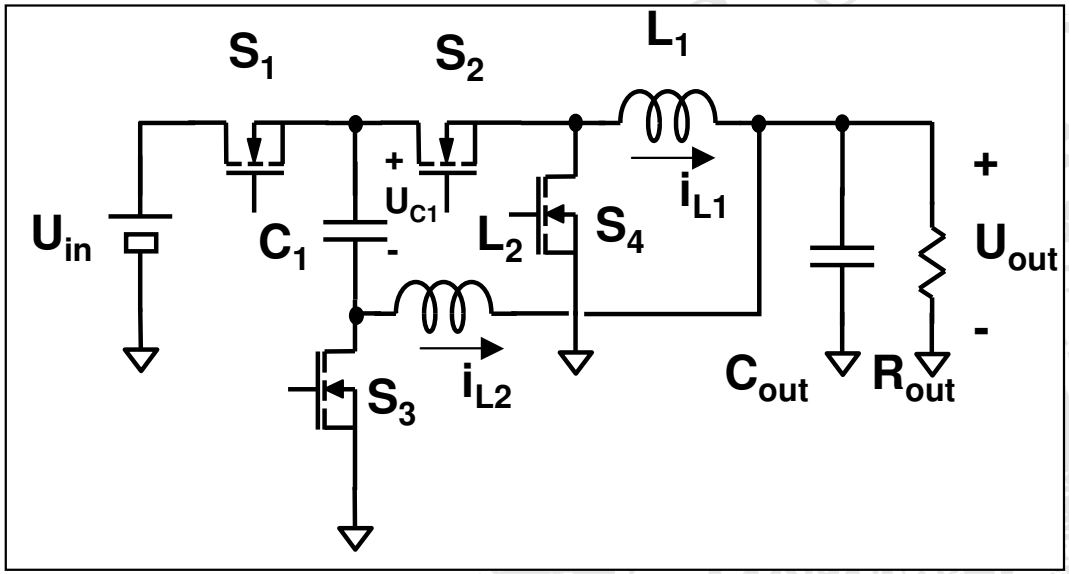
Topologies for POL converters



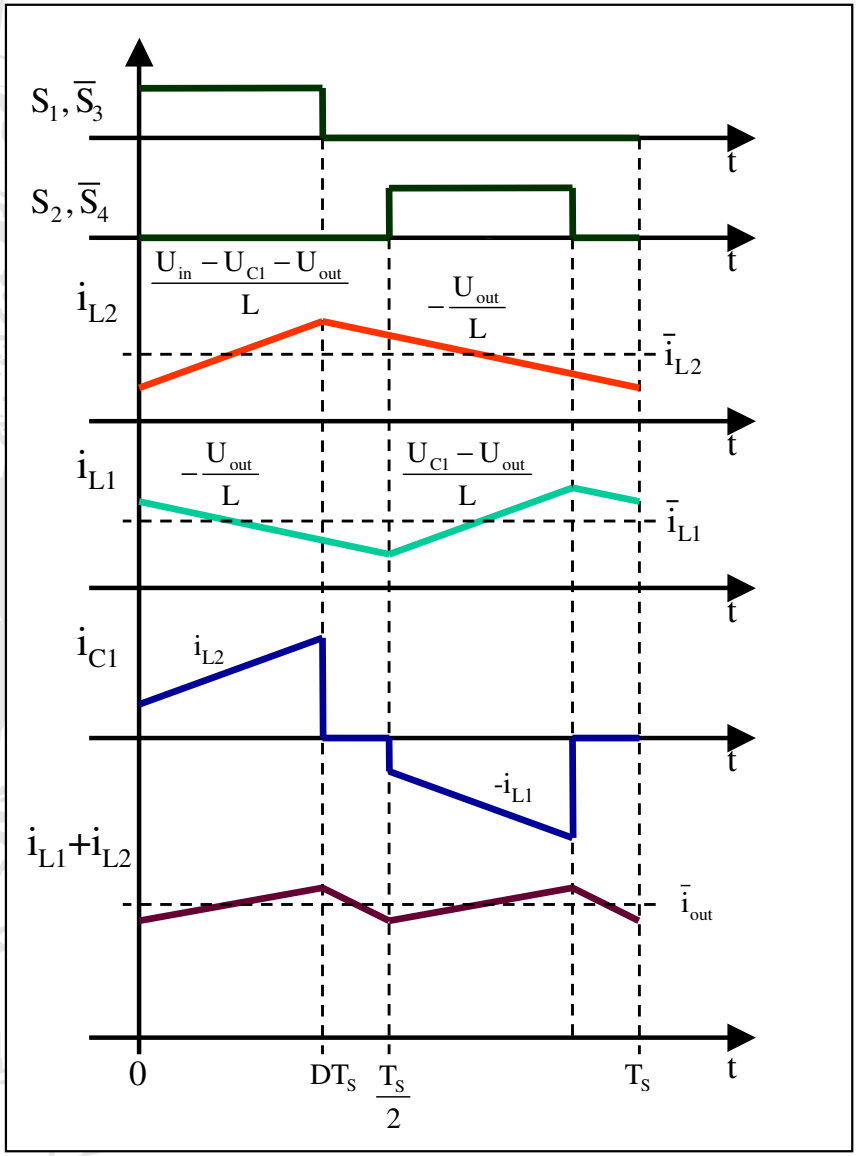
Topologies for POL converters

- Converter analysis and key waveforms determination.
- Preliminary design based on basic specifications, considering:
  - different switching frequencies;
  - different operating modes (CCM versus QSW).
- Calculation of average, peak and RMS currents in the switches and inductors.
- Tentative efficiency estimation, including also:
  - switching losses (by SPECTRE simulations of switch commutations);
  - skin and proximity effects.

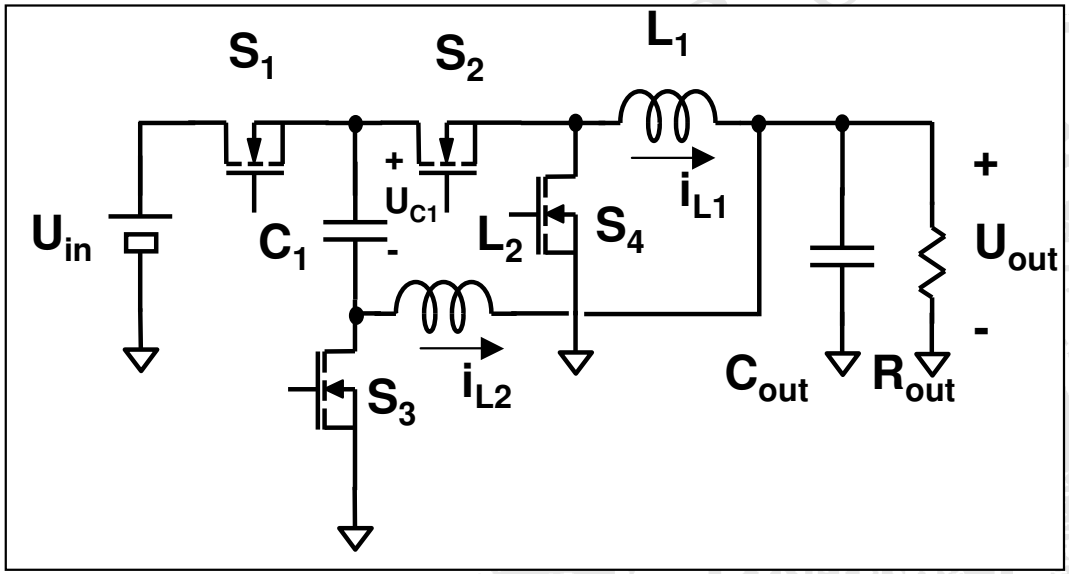
2PBIVD converter

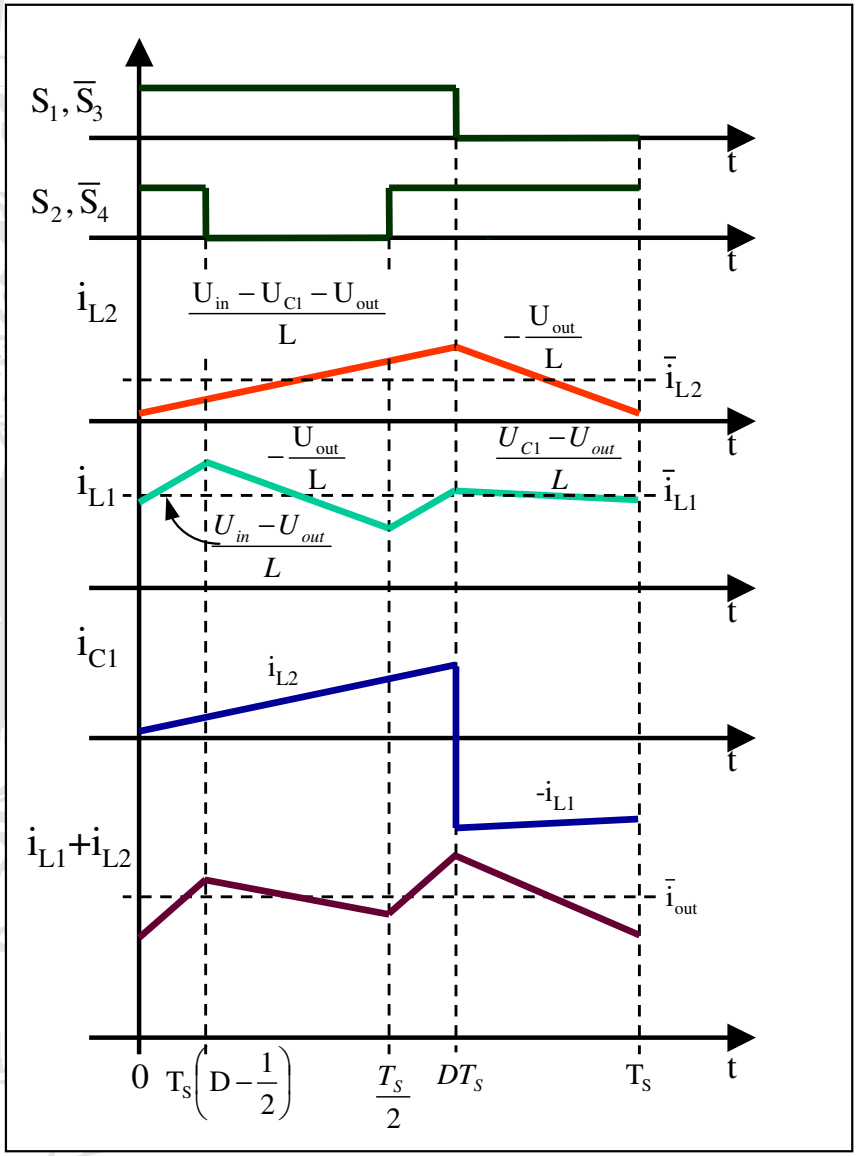


$0 < D < 0.5$



2PBIVD converter





0.5 < D < 1

2PBIVD converter

Key steady state equations: voltage conversion ratios

$$\frac{U_{out}}{U_{in}} = \begin{cases} \frac{D}{2} & if \quad D < 0.5 \\ D^2 & if \quad D \geq 0.5 \end{cases} \qquad \frac{U_{C1}}{U_{in}} = \begin{cases} \frac{1}{2} & if \quad D < 0.5 \\ 1-D & if \quad D \geq 0.5 \end{cases}$$

Key steady state equations: current sharing

$$D \leq 0.5 \Rightarrow \qquad \bar{I}_{L1} = \bar{I}_{L2} = \frac{I_{out}}{2}$$

$$D > 0.5 \Rightarrow \qquad \bar{I}_{L1} = D \cdot I_{out}, \qquad \bar{I}_{L2} = (1-D) \cdot I_{out}$$

2PBIVD converter

Key dynamic equation: duty-cycle to output voltage transfer function

$$G_{ud}(s) = \frac{U_{in}}{2} \frac{1 + \frac{LC_1}{2D^2} s^2}{\left(1 + \frac{LC_1}{2D^2} s^2\right)\left(1 + \frac{L}{2R_{out}} s + \frac{LC_{out}}{2} s^2\right)} =$$

$$= \frac{U_{in}}{2} \frac{1}{1 + \frac{L}{2R_{out}} s + \frac{LC_{out}}{2} s^2}$$

2PBIVD converter

2PBIVD efficiency estimation with the considered CMOS technology

		f_S [MHz]					
		1*	2	2*	3*	5*	5
Inductance [nH]		400	400	200	100	80	200
R_{DSon} [mΩ]	10	0.892	0.899	0.907	0.893	0.884	0.866
	20	0.888	0.901	0.907	0.895	0.885	0.878
	50	0.869	0.888	0.889	0.874	0.883	0.873
	100	0.836	0.862	0.855	0.833	0.852	0.851
	200	0.776	0.813	0.792	0.761	0.791	0.806
	500	0.638	0.694	0.649	0.602	0.648	0.693

The shaded rows correspond to the expected R_{DSon} values. * indicates QSW operation.

Design example

Synchronous Buck Power Stage Parameters

Input capacitor	**C_{in}**	**100nF + 10μF**
Output capacitor	**C_o**	**2x47nF +2x47μF + 2x10μF**
Phase inductance	**L**	**220nH – 50mΩ**
Power switches	**$S_{1,2}$**	**2xIRF8915**

Converters are designed for QSW operation

Design example

Synchronous Buck Power Stage Parameters		
Interleaved Buck Power Stage Parameters		
Input capacitor	**C_{in}**	**100nF + 10μF**
Output capacitor	**C_o**	**2x47nF + 4x10μF**
Phase inductance	**L_1**	**353nH – 90mΩ**
Phase inductance	**L_2**	**342nH – 86mΩ**
Power switches	**$S_{1,..4}$**	**4xIRF8915**

Converters are designed for QSW operation

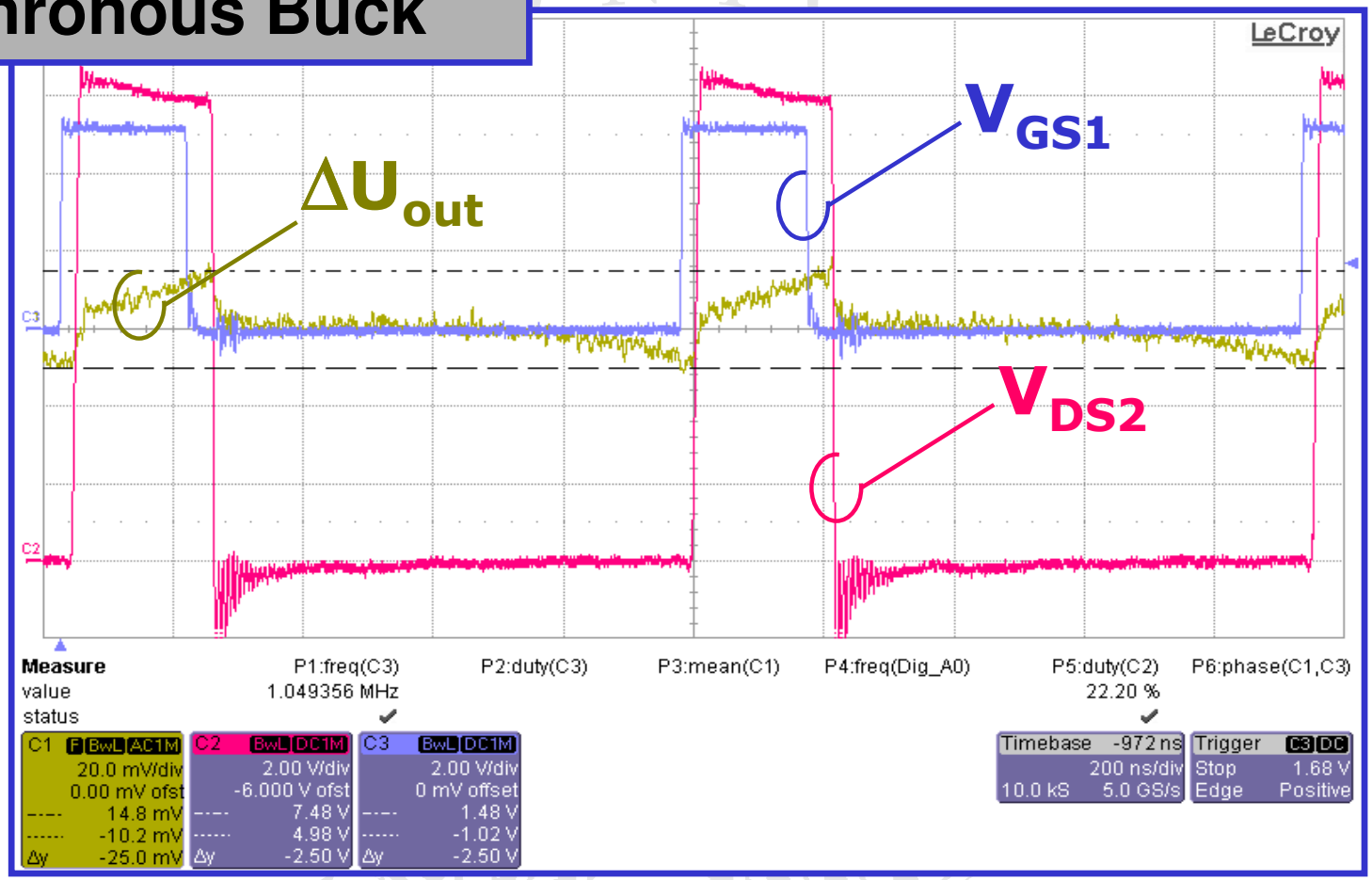
Design example

Synchronous Buck Power Stage Parameters		
Interleaved Buck Power Stage Parameters		
2PBIVD Power Stage Parameters		
Input capacitor	C_{in}	100nF + 10μF
Energy transfer capacitor	C_1	2x470nF
Output capacitor	C_o	2x47nF + 4x2.2μF
Phase inductance	L_1	353nH – 90mΩ
Phase inductance	L_2	342nH – 86mΩ
Power switches	$S_{1,..4}$	4xIRF8915

Converters are designed for QSW operation

Experimental tests: waveforms

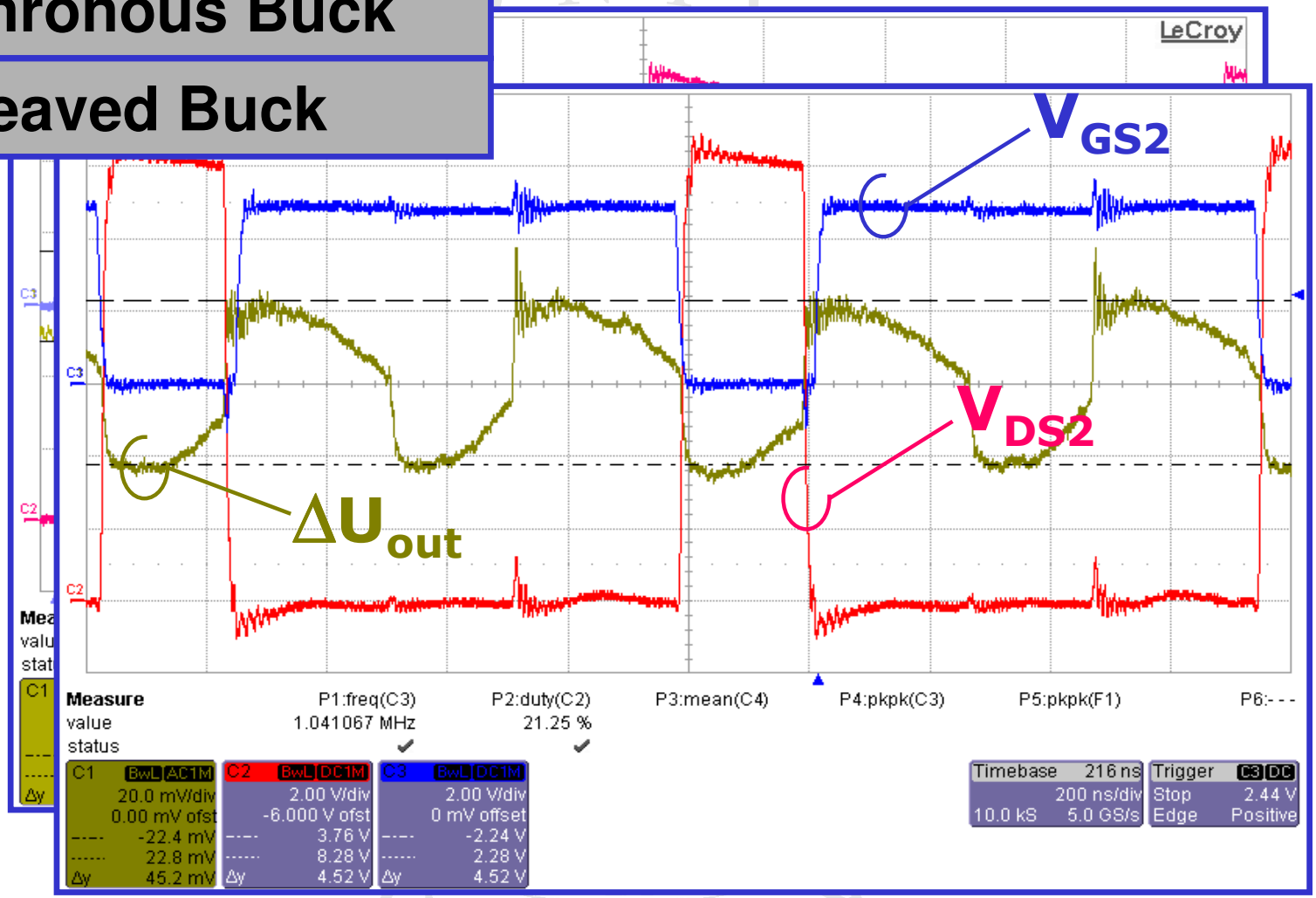
Synchronous Buck



Experimental tests: waveforms

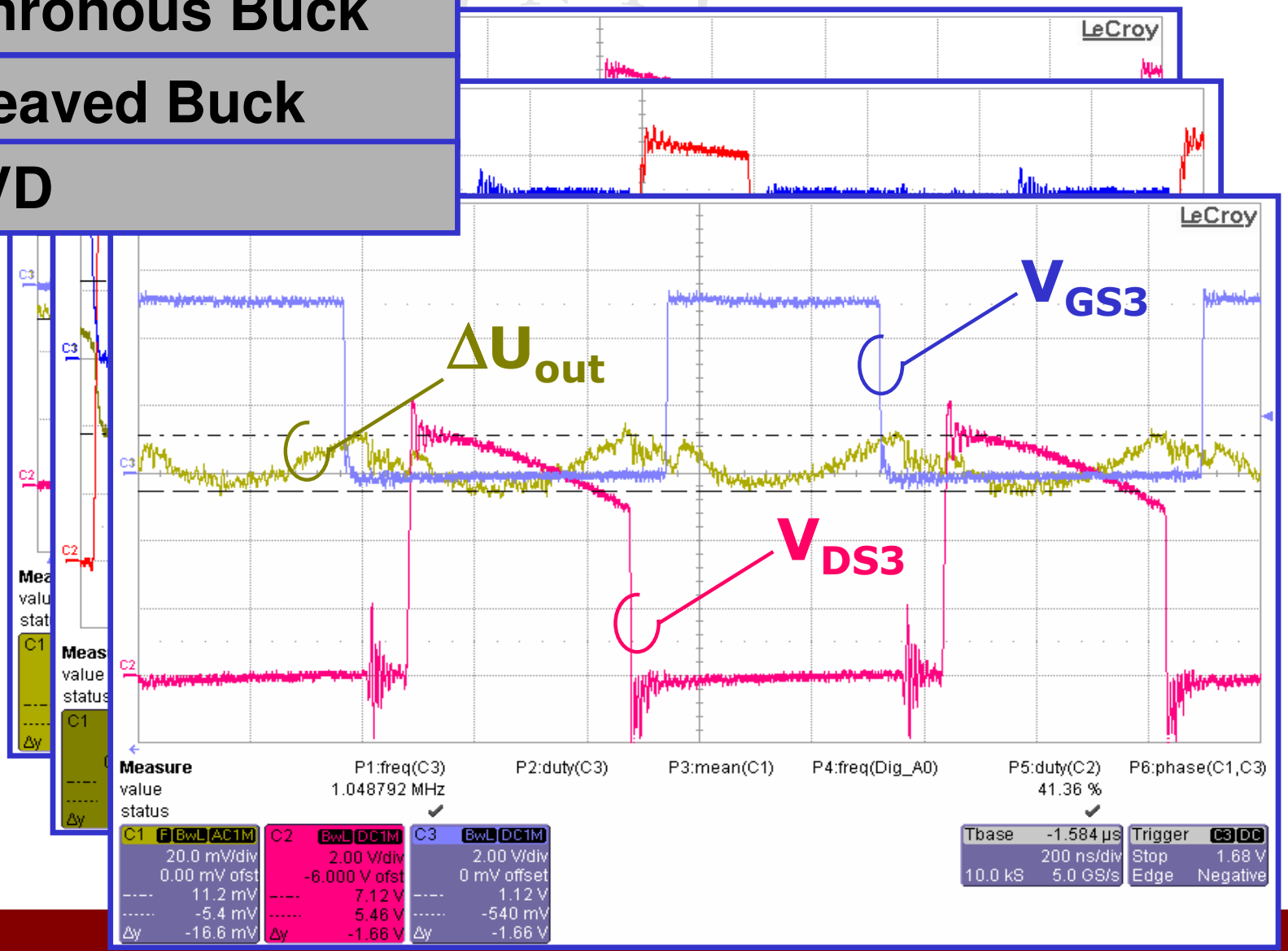
Synchronous Buck

Interleaved Buck



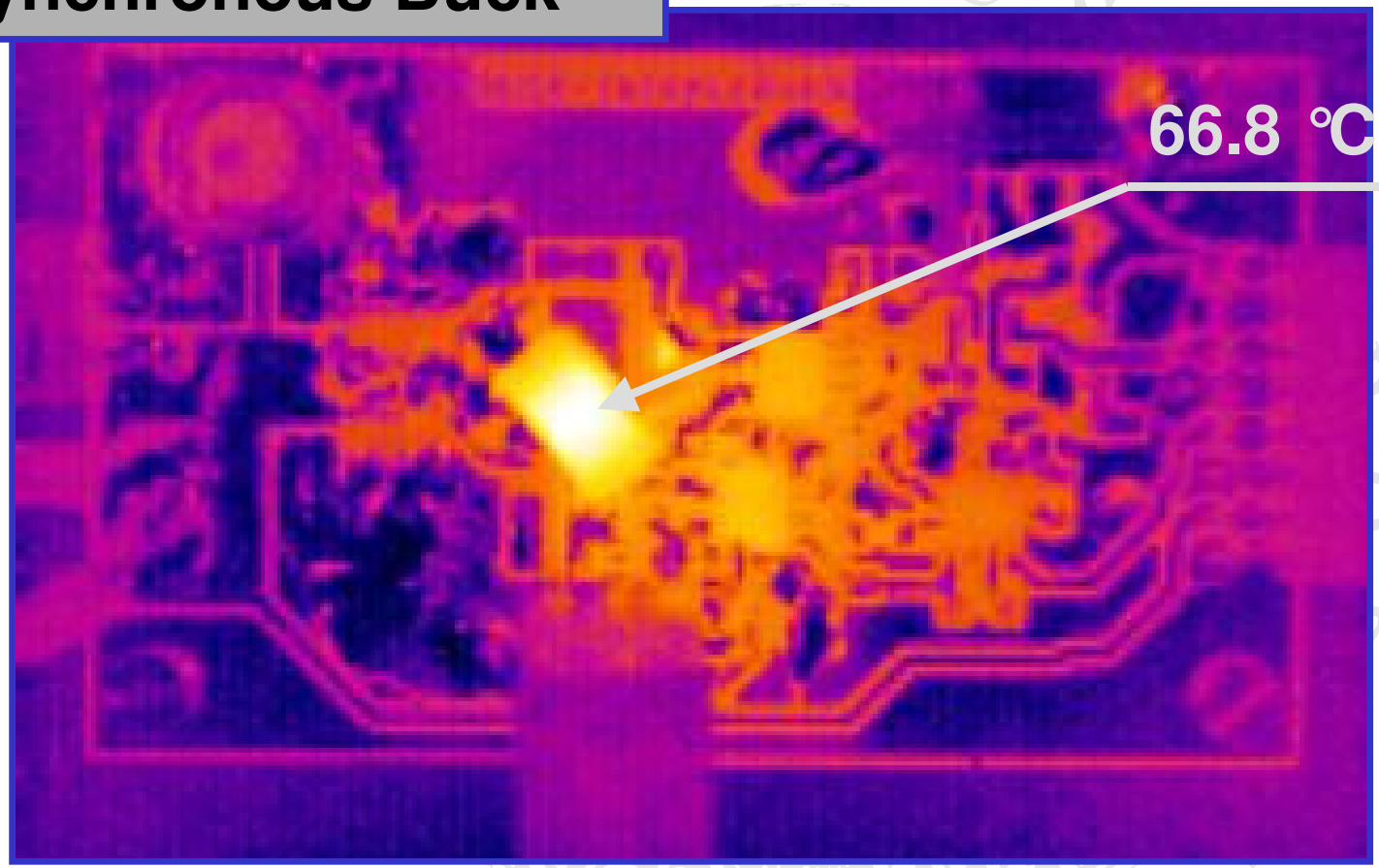
Experimental tests: waveforms

- Synchronous Buck
- Interleaved Buck
- 2PBIVD



Experimental tests: thermal analysis

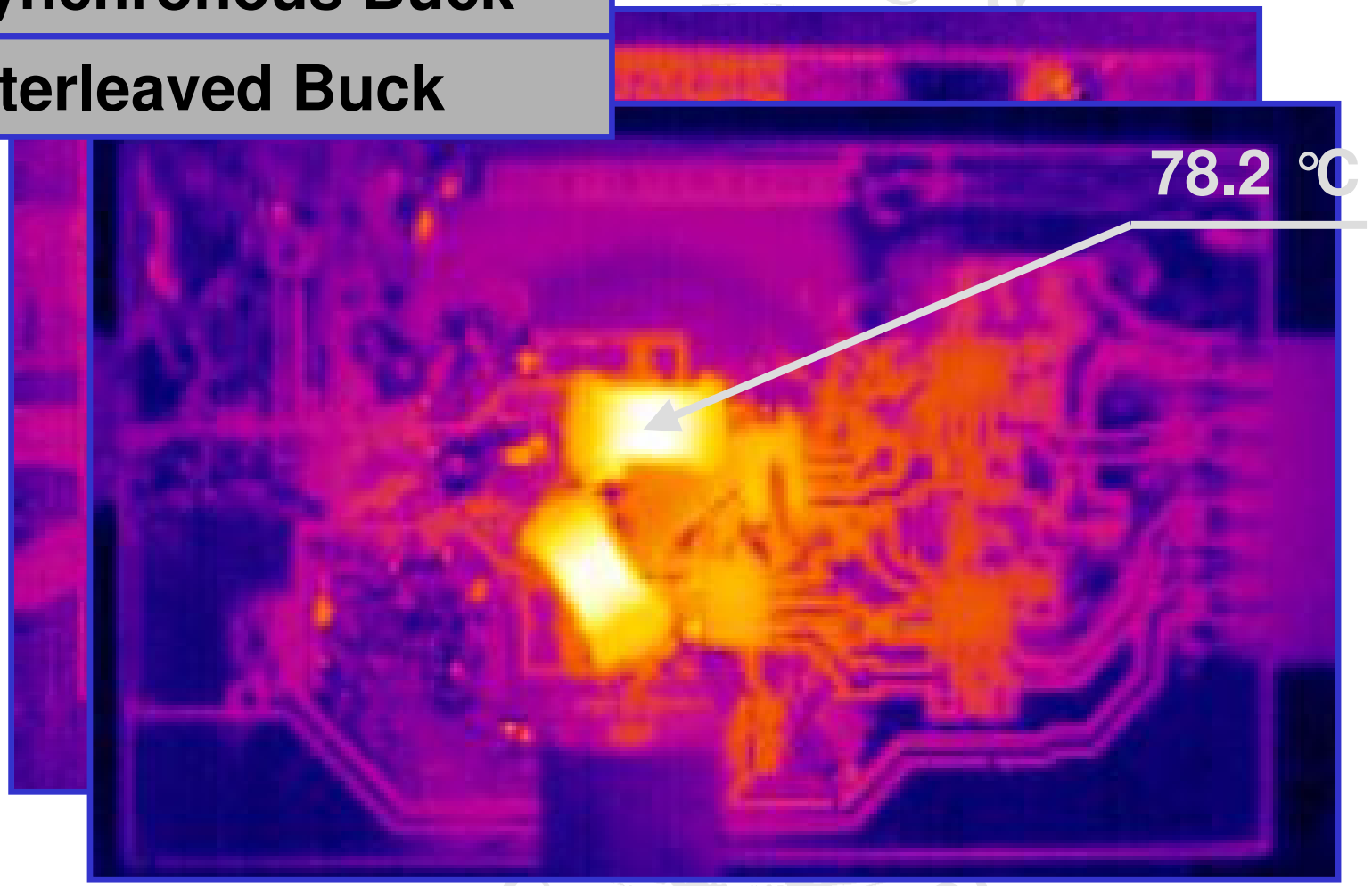
Synchronous Buck



Experimental tests: thermal analysis

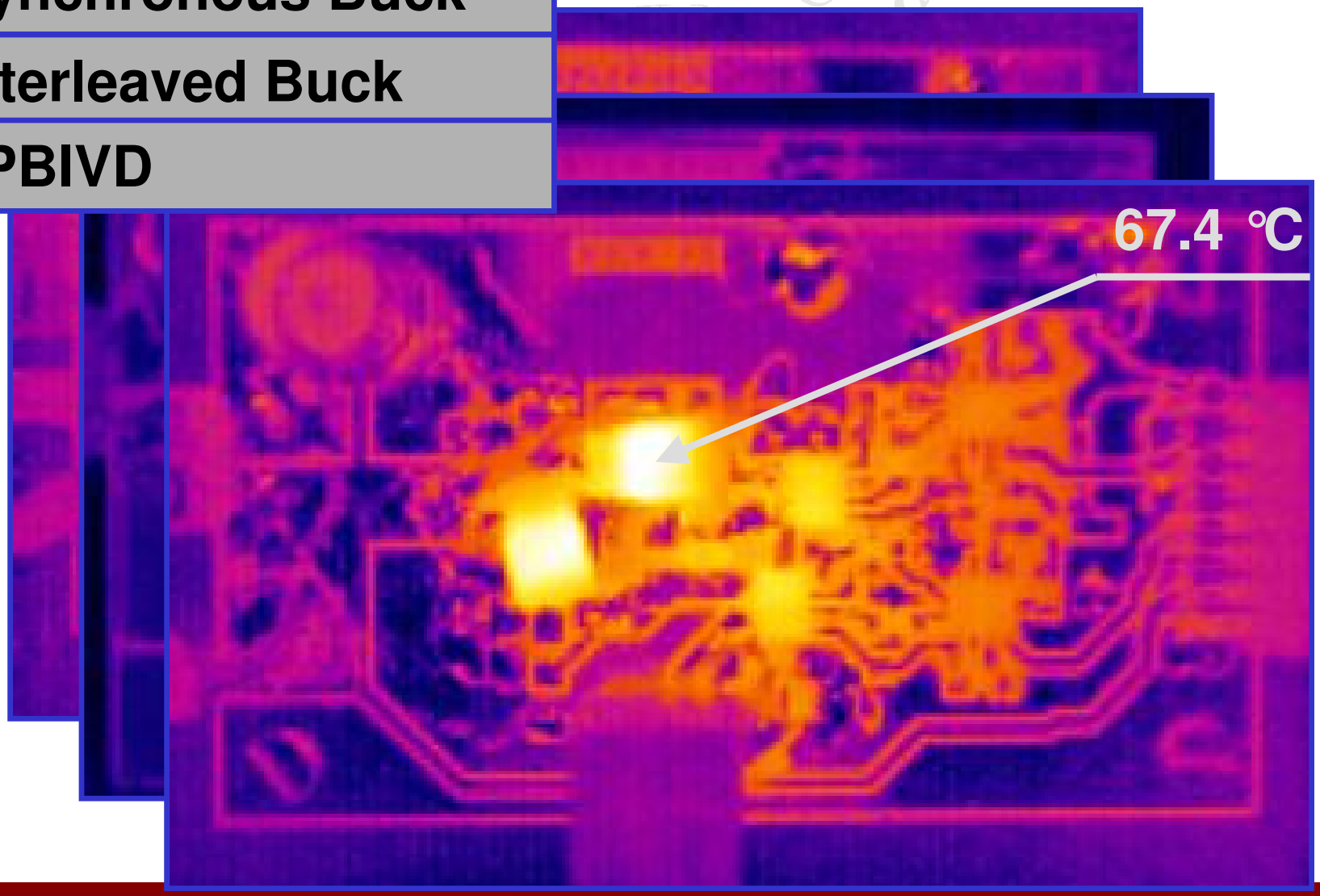
Synchronous Buck

Interleaved Buck



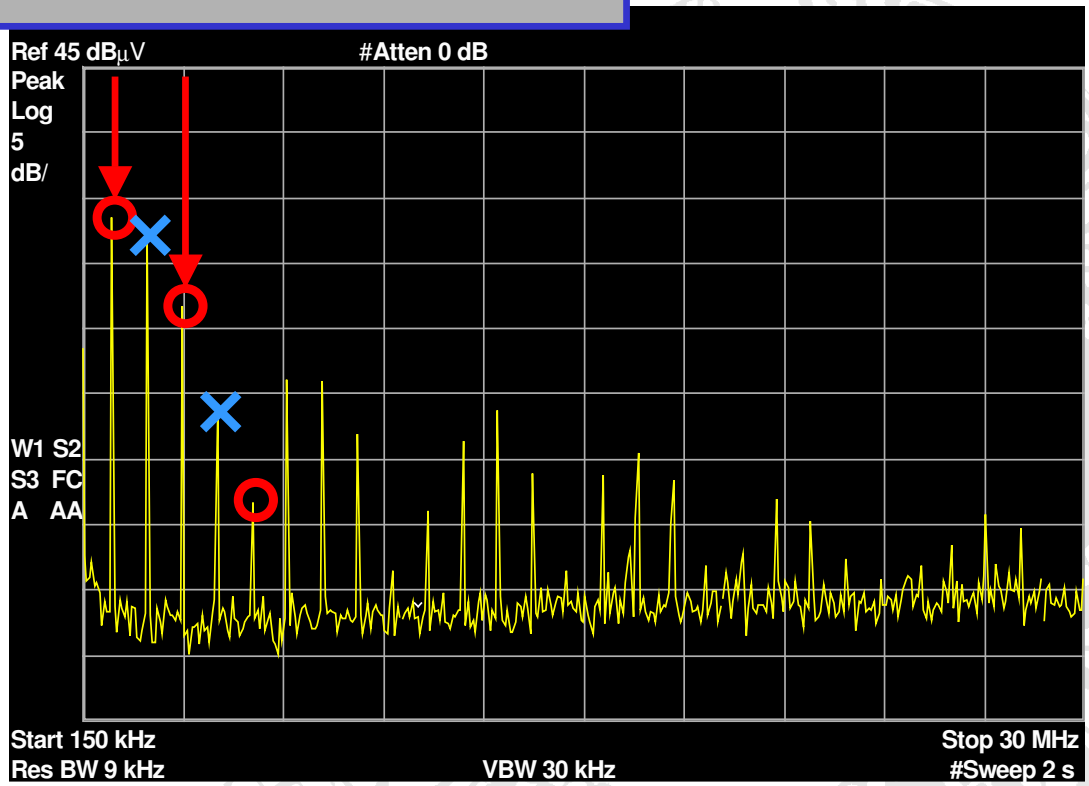
Experimental tests: thermal analysis

- Synchronous Buck
- Interleaved Buck
- 2PBIVD



Experimental tests: conducted DM noise

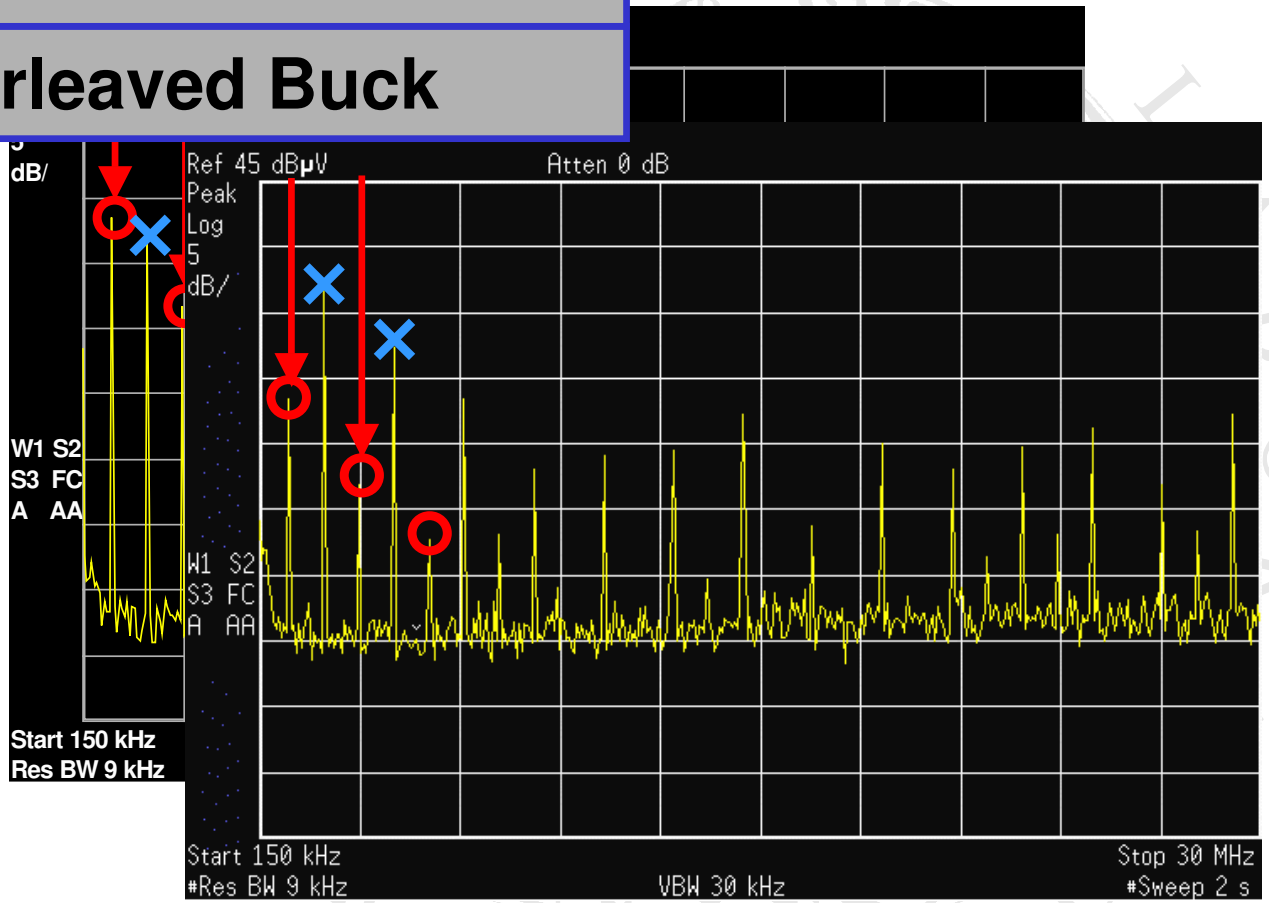
Synchronous Buck



Experimental tests: conducted DM noise

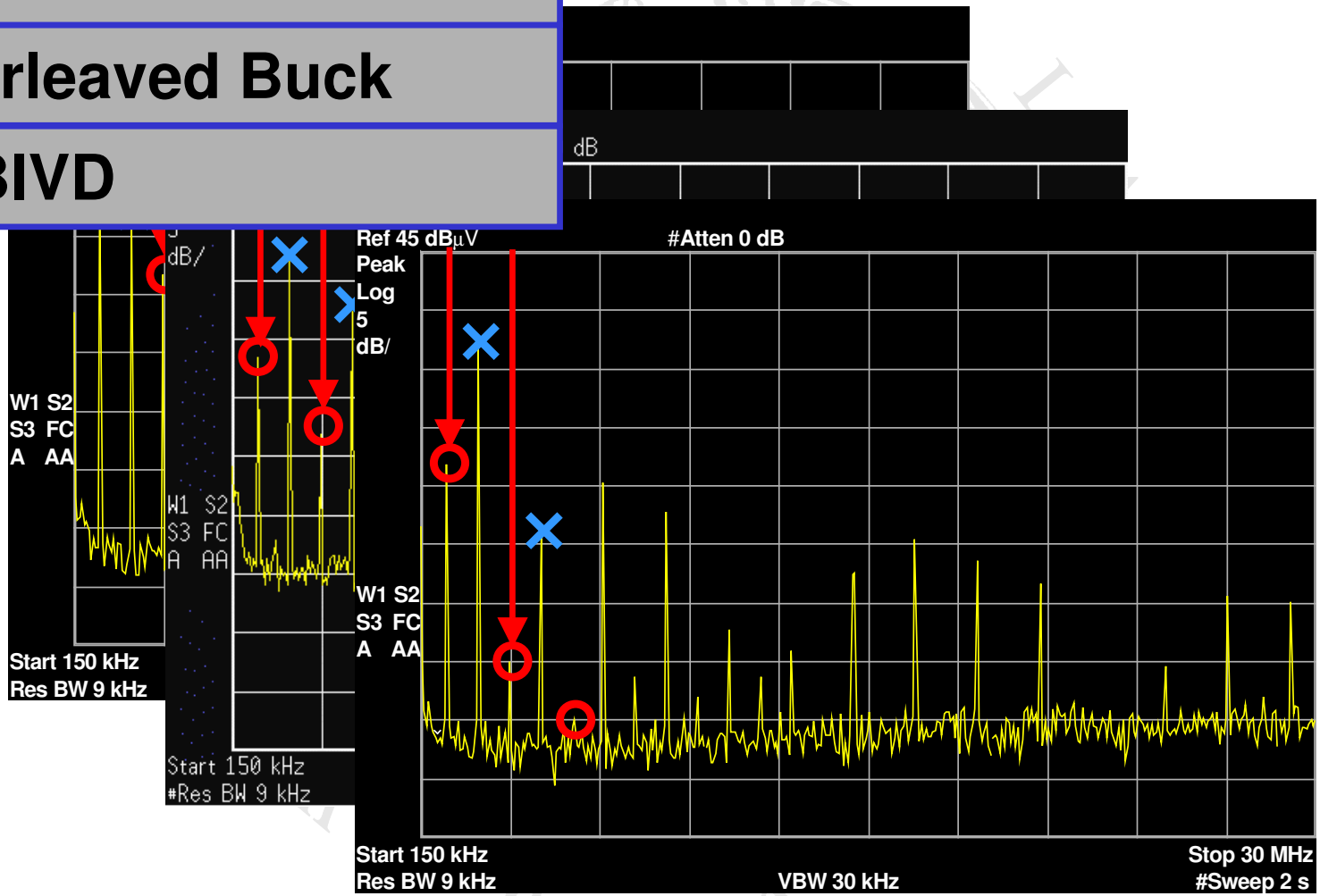
Synchronous Buck

Interleaved Buck



Experimental tests: conducted DM noise

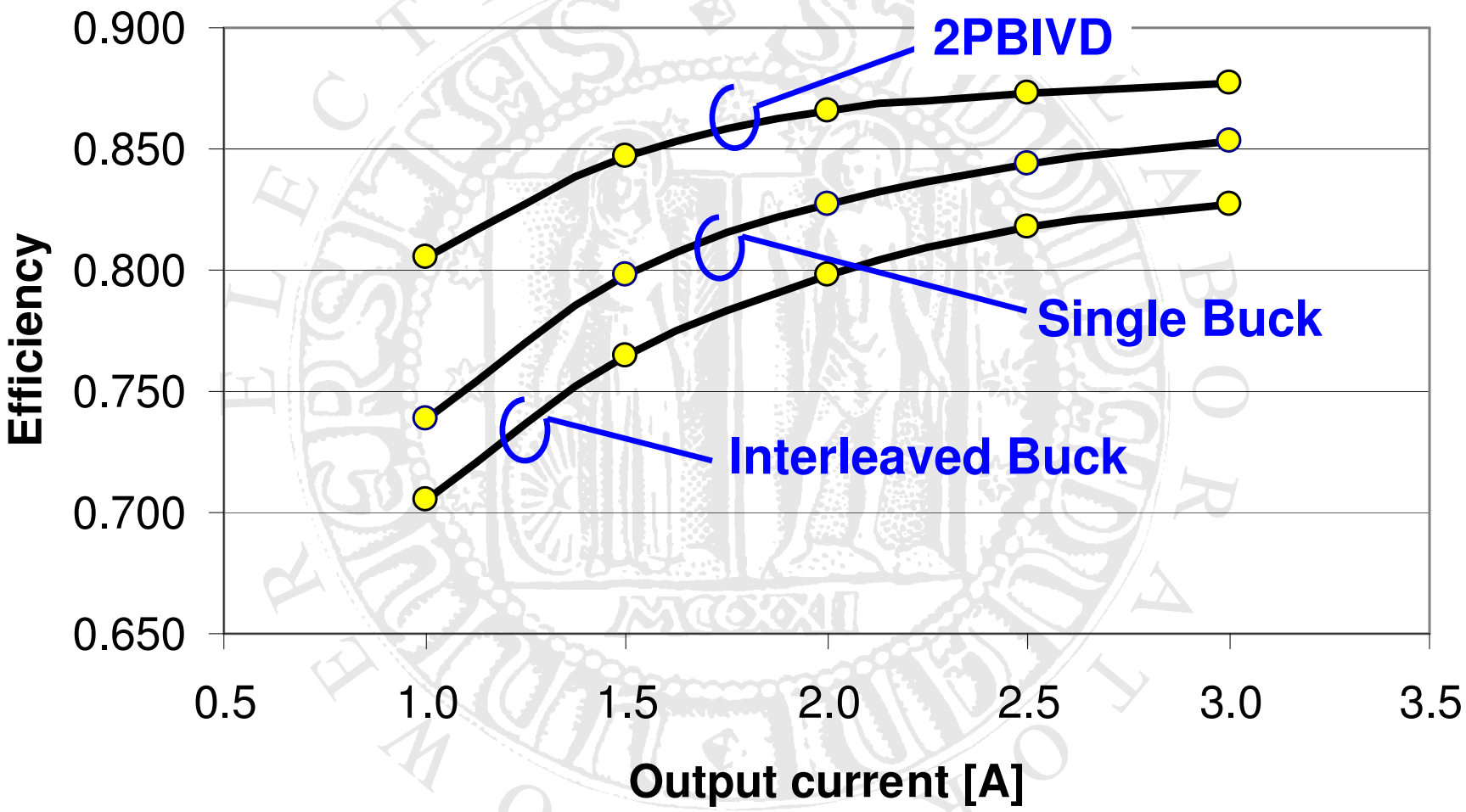
- Synchronous Buck
- Interleaved Buck
- 2PBIVD



Experimental tests: efficiency

I_o [A]	Efficiency		
	Single Buck	Interleaved Buck	2PBIVD
3.0	0.853	0.827	0.877
2.5	0.844	0.818	0.873
2.0	0.827	0.798	0.866
1.5	0.798	0.765	0.847
1.0	0.739	0.705	0.805

Experimental tests: efficiency



Experimental tests: outcome

- **The 2PIBVD converter offers a measurable advantage in terms of switch voltage stress and output capacitance values and efficiency with respect to the simple buck converter and the conventional two phase interleaved converter.**

- **Thermal and electromagnetic noise behaviors are comparable, but, as far as noise is concerned, the interleaved solutions are preferable.**

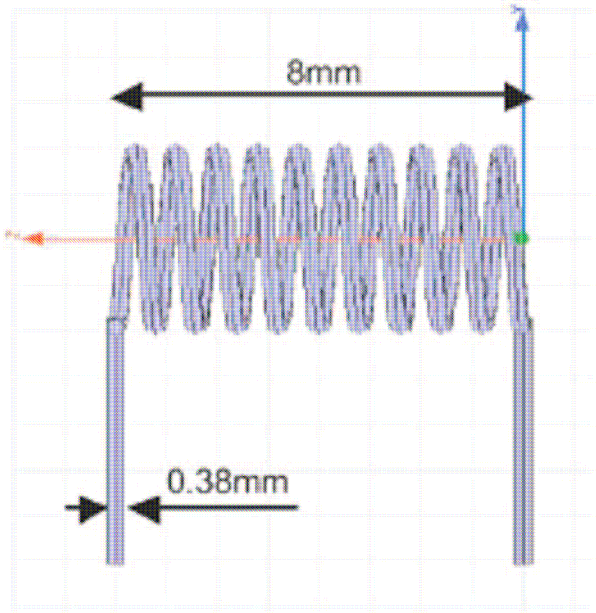
Converter on chip implementation

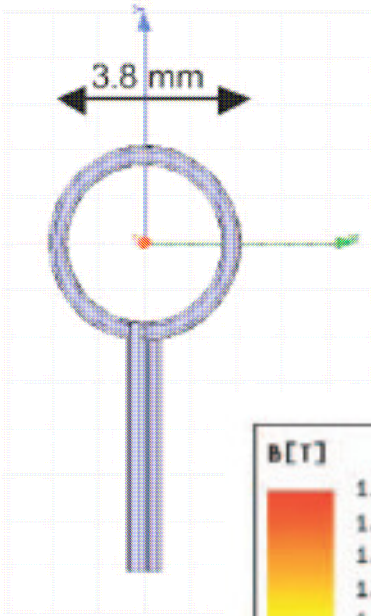
Phase 3 **of the research is the *on chip* implementation and test of the point of load converter.**

The air core inductor has to be designed and optimized for minimum size and minimum leakage flux (to minimize interference with sensor electronics).

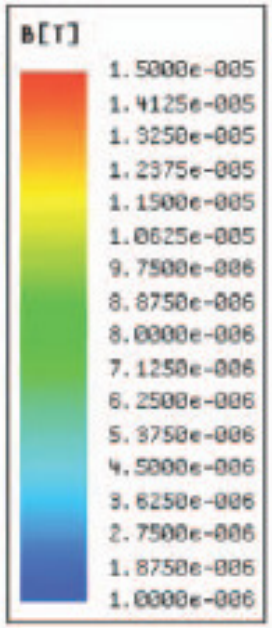
Two different solutions have been considered and compared.

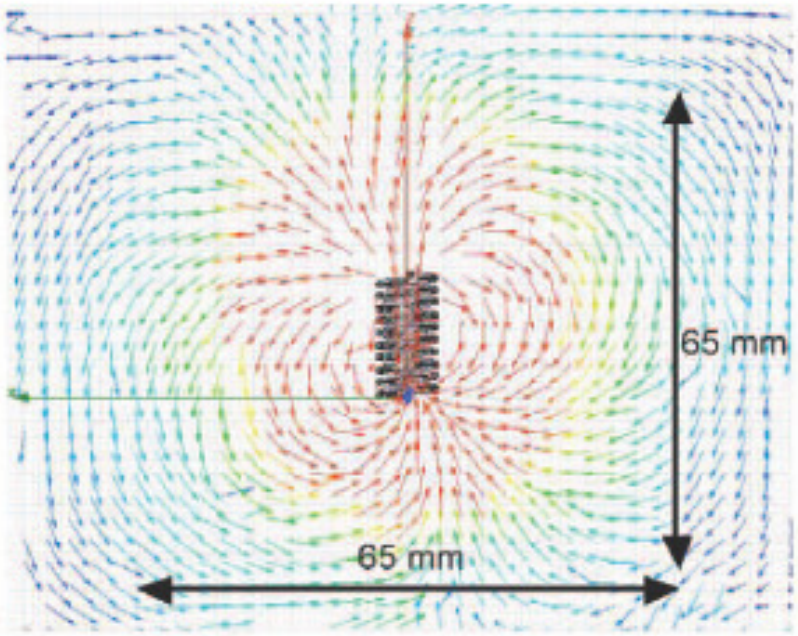
Inductor implementation



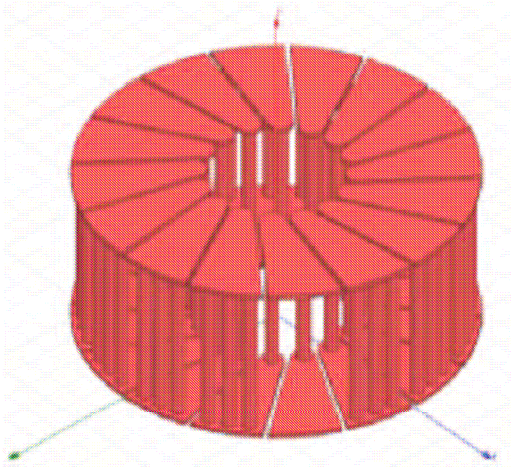


Solenoidal air core inductor

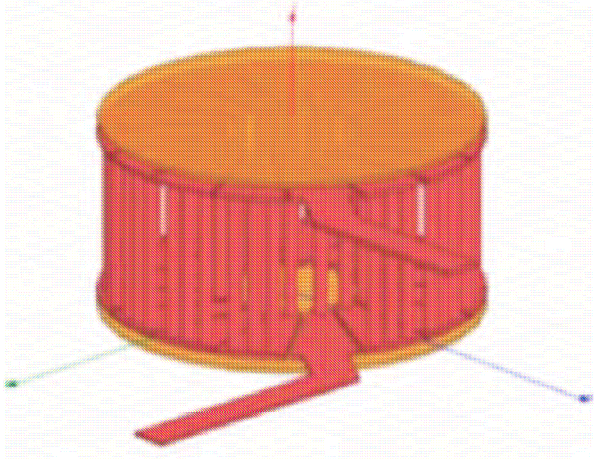




Inductor implementation

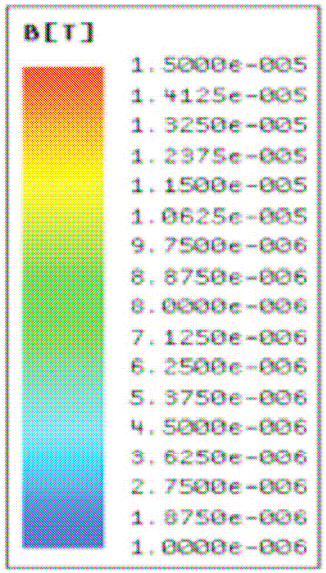


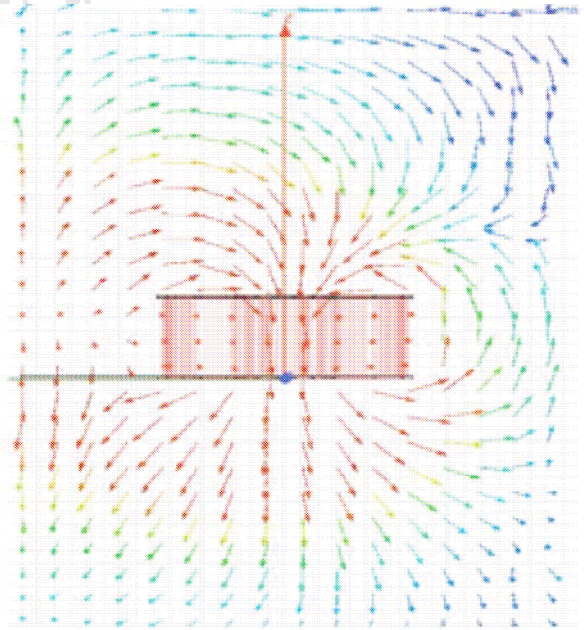
(a) PCB toroid



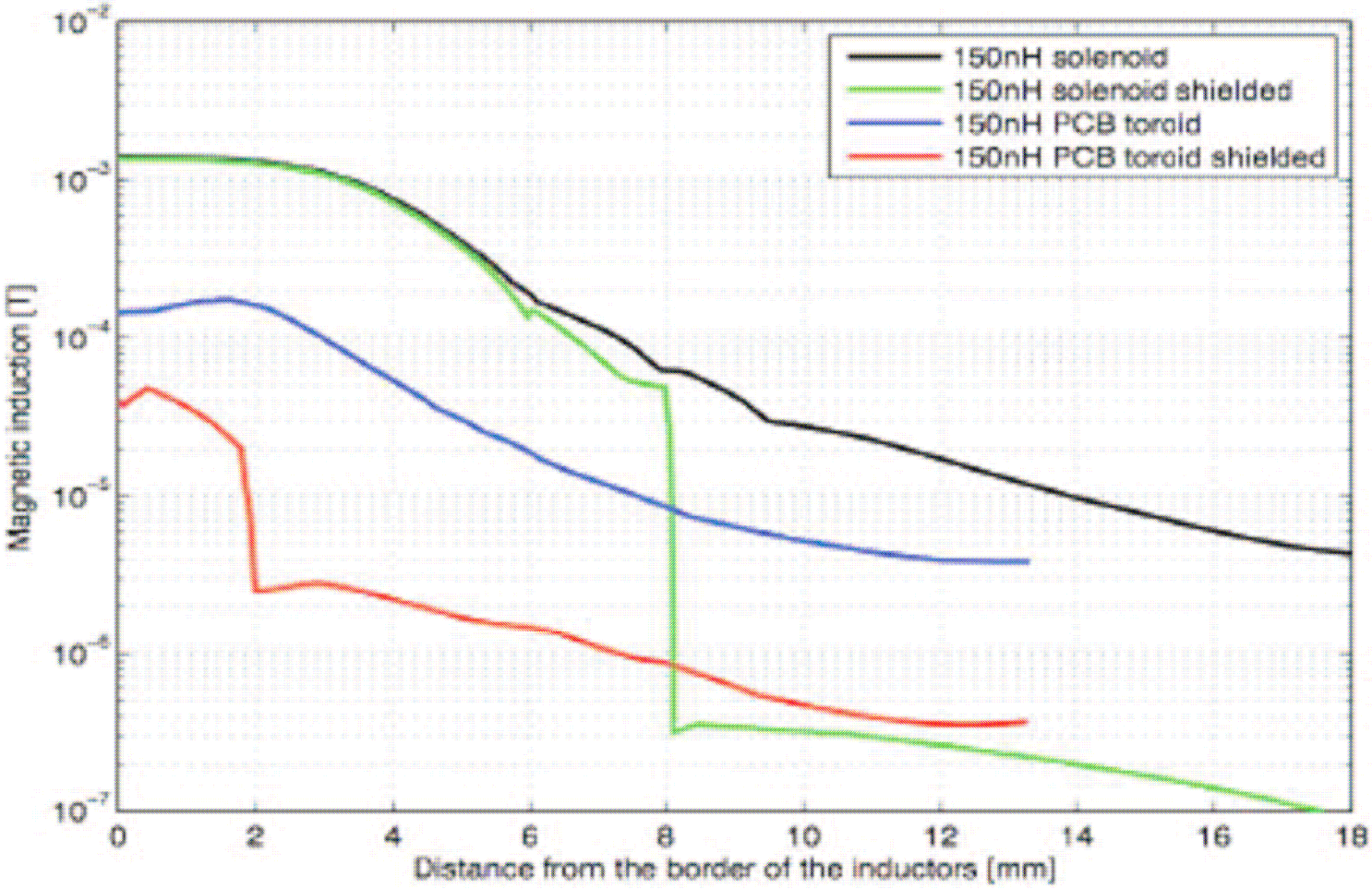
(b) Shielded PCB toroid

Toroidal air core inductor





Inductor implementation



z-axis magnetic induction

Inductor implementation

PCB air-core toroidal inductors seem to be a good solution, showing reduced values of series resistance (comparable to those of an equivalent solenoid), well confined magnetic field and the possibility of being shielded without reducing the inductance value.

Nevertheless, the electrical performance of the PCB toroid relies on the use of copper filled vias, that are difficult to manufacture and that can present some reliability problems.

An alternative to this approach consists on custom wrapped air-core toroidal inductors.

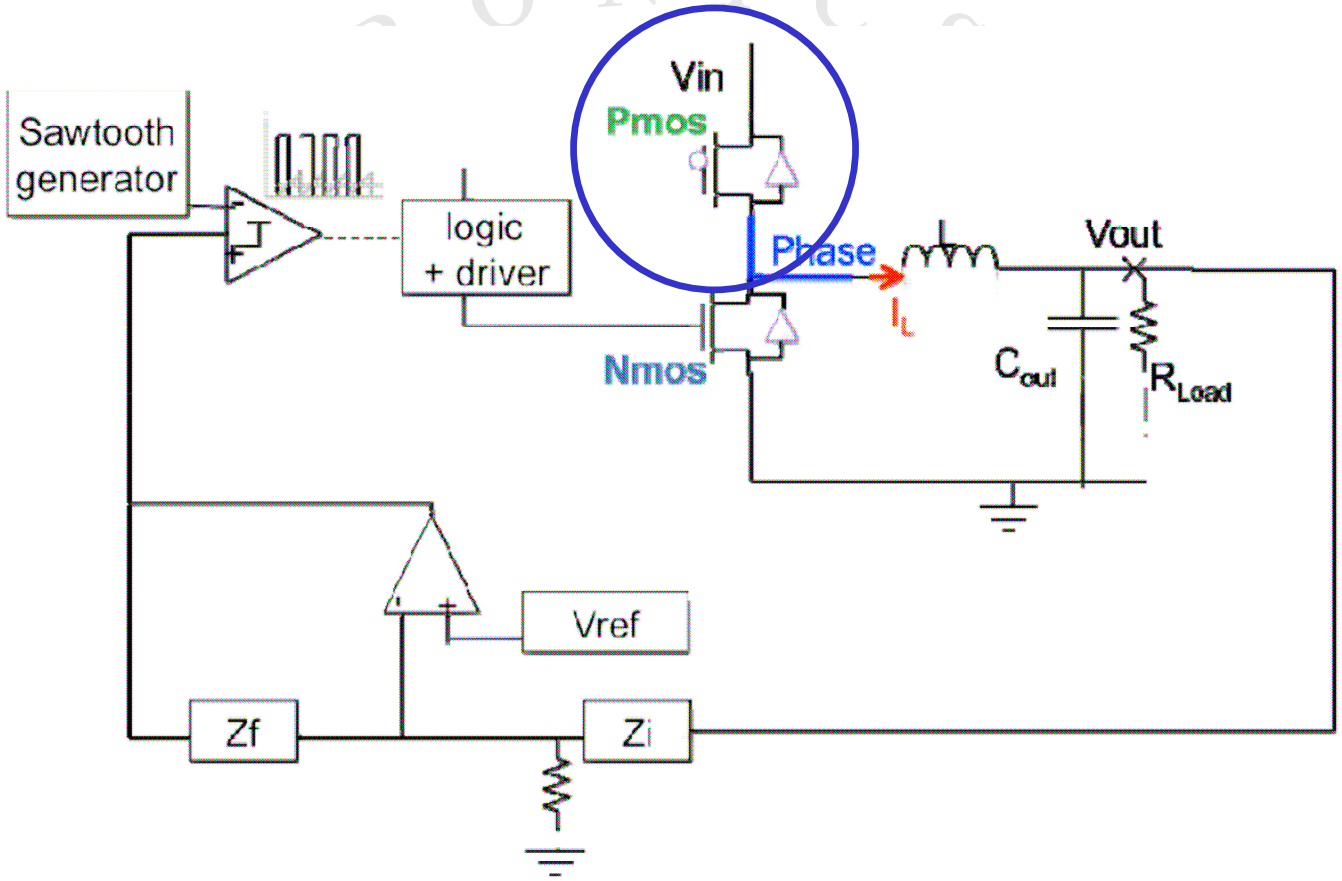
Circuit on chip implementation

As a first experiment, a simple Buck converter configuration was implemented on-chip, so as to test the technology in a basic circuit configuration.

Converter design has been performed in the 0.25µm SGB25GOD technology from IHP (Innovations for High Performance microelectronics, Frankfurt Oder, Germany) that shows good radiation hardness and electrical performance.

To maximize efficiency, careful selection of switch size is required. Additionally, dead time duration can be adapted to optimise QSW operation.

Circuit on chip implementation



On chip synchronous buck with CMOS arrangement

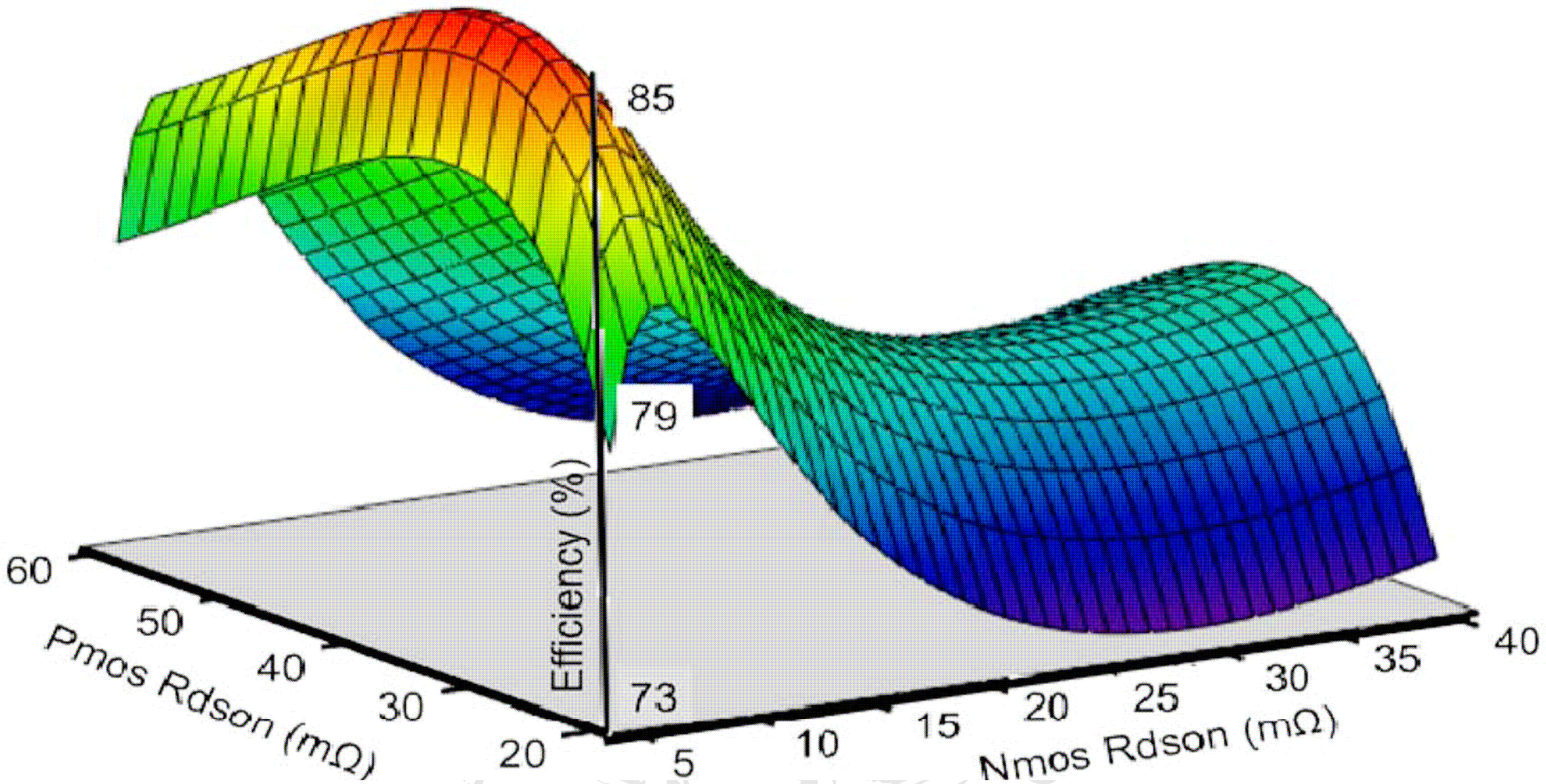
Circuit on chip implementation

Based on detailed simulations of the switch commutations (different from the usual inductive load ones), the converter efficiency can be estimated and its relation with the NMOS and PMOS sizes can be investigated.

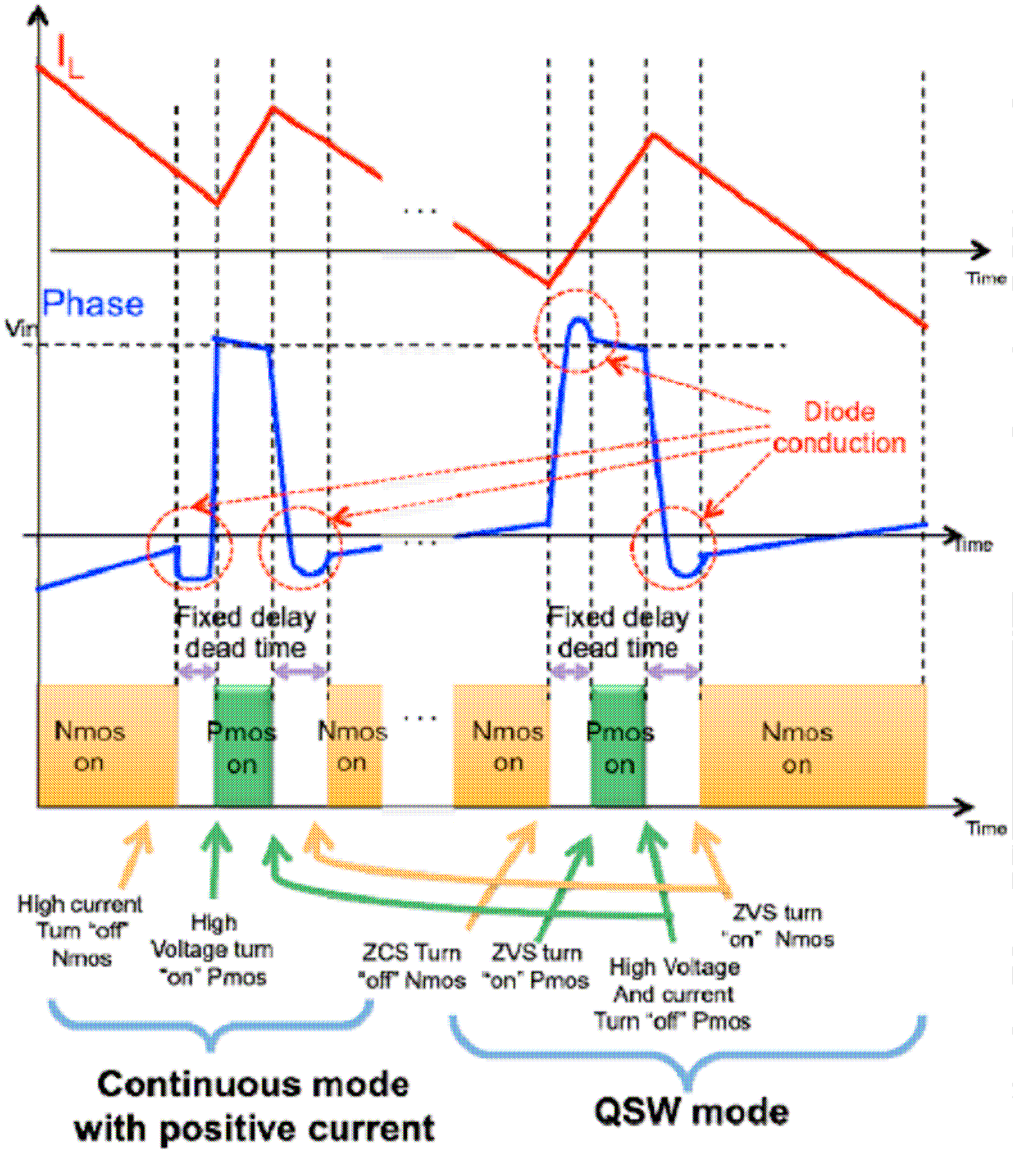
It is important to remember that *increasing* the switch channel width W *reduces* the R_{DSon} (which is good), but *increases* the parasitic capacitance (which is bad).

An optimal size can be identified, that maximizes the overall conversion efficiency. Typical W values are around 0.25 m.

Circuit on chip implementation



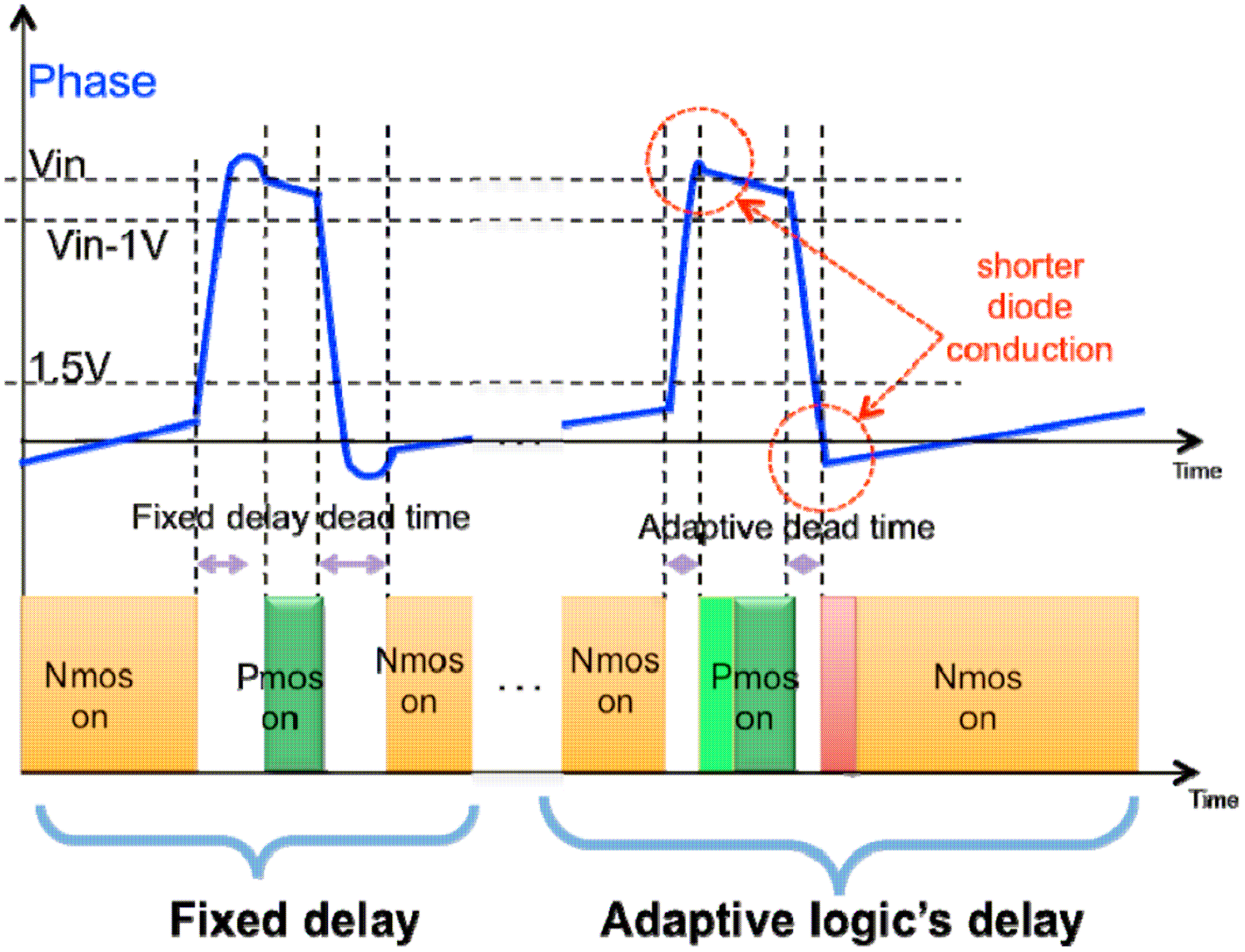
Circuit on chip implementation



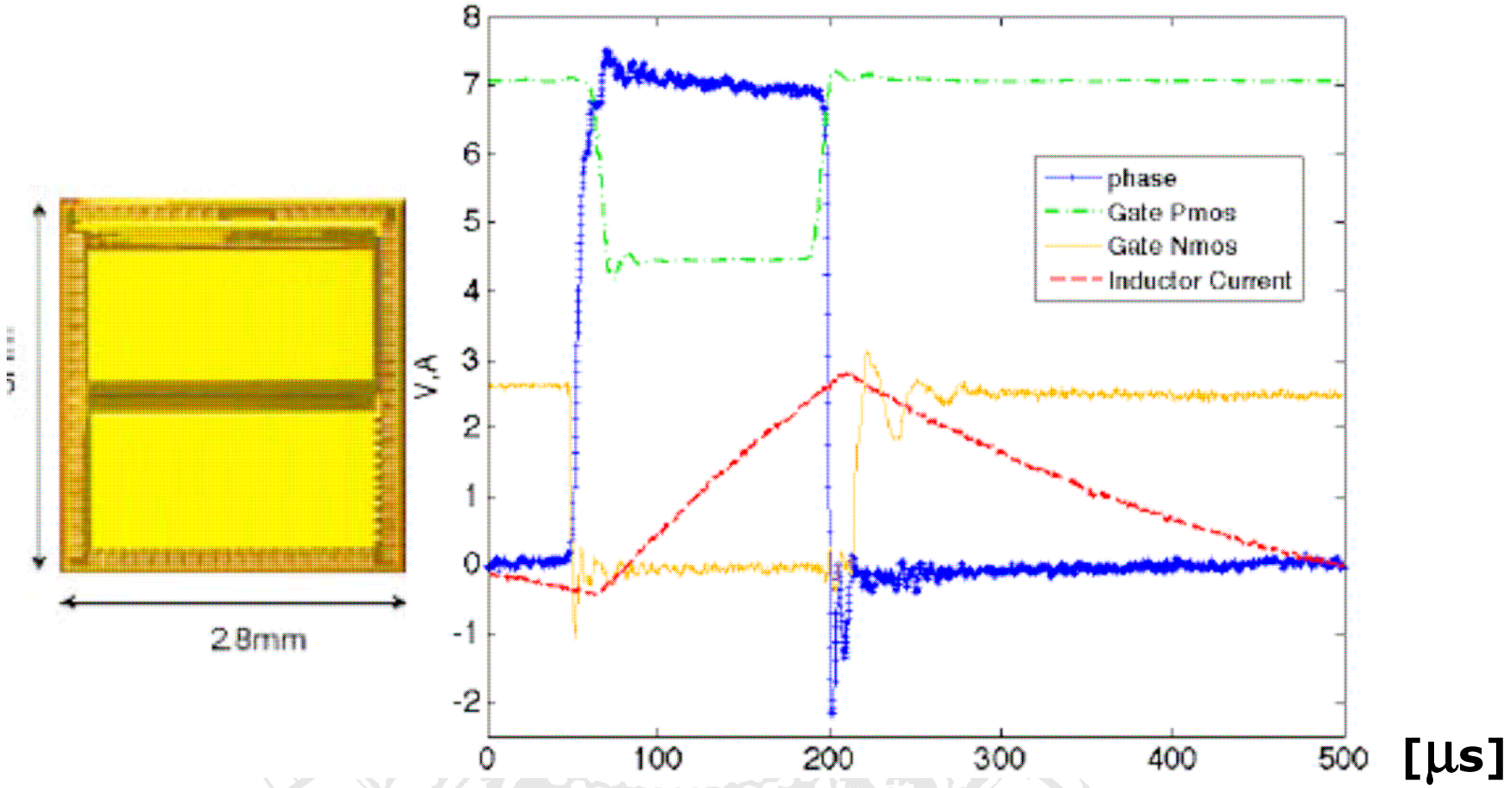
QSW mode with small negative I_L allows having three soft commutations out of four. Its drawback is however the increased ripple of the inductor current, which originates more relevant conduction losses.

Overall, given the target f_s above 1 MHz, the QSW mode gives the best estimated performance in our application. To further reduce the losses, a dedicated circuit was introduced that dynamically reduces the dead time to the minimum.

Circuit on chip implementation

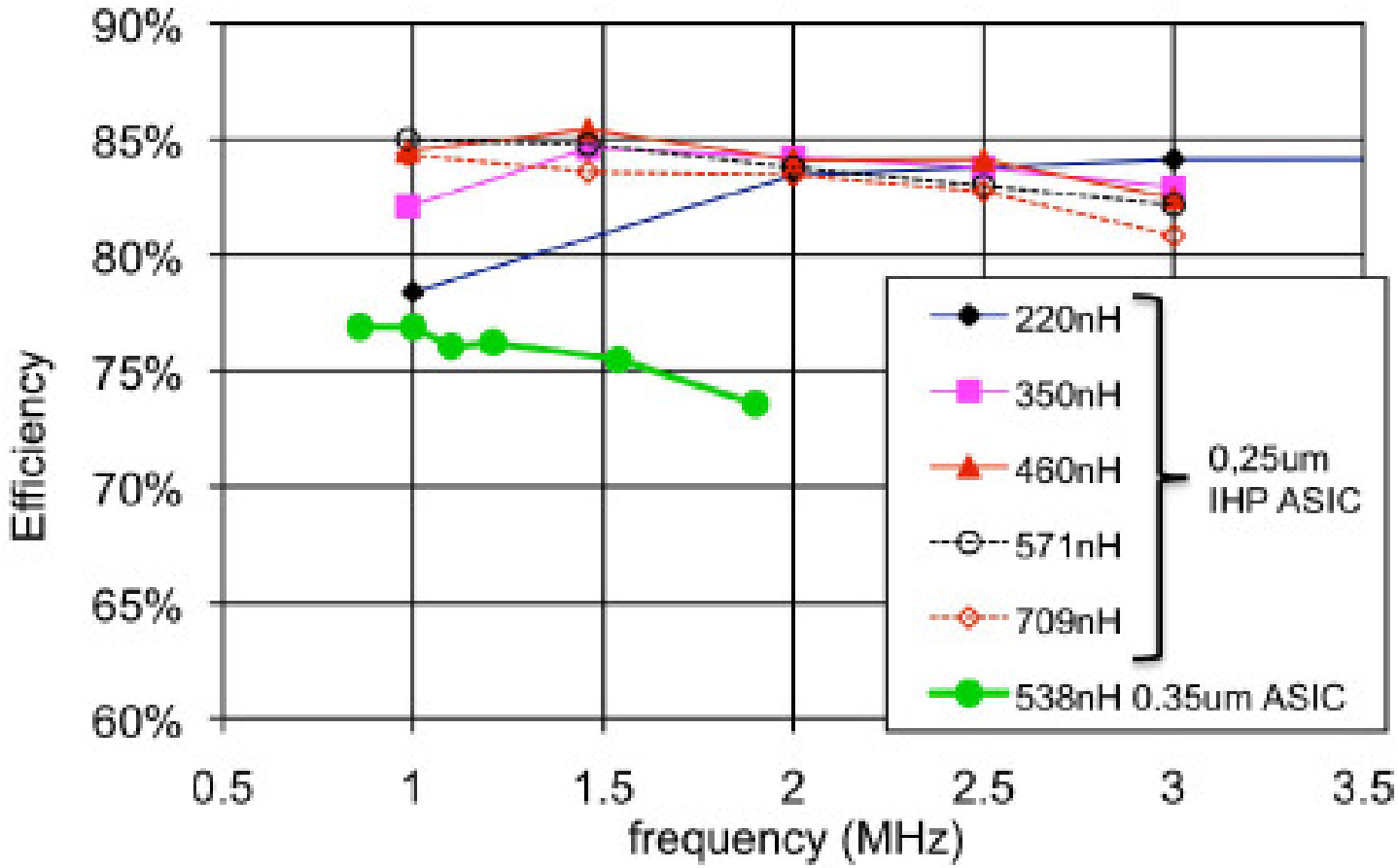


Circuit on chip implementation



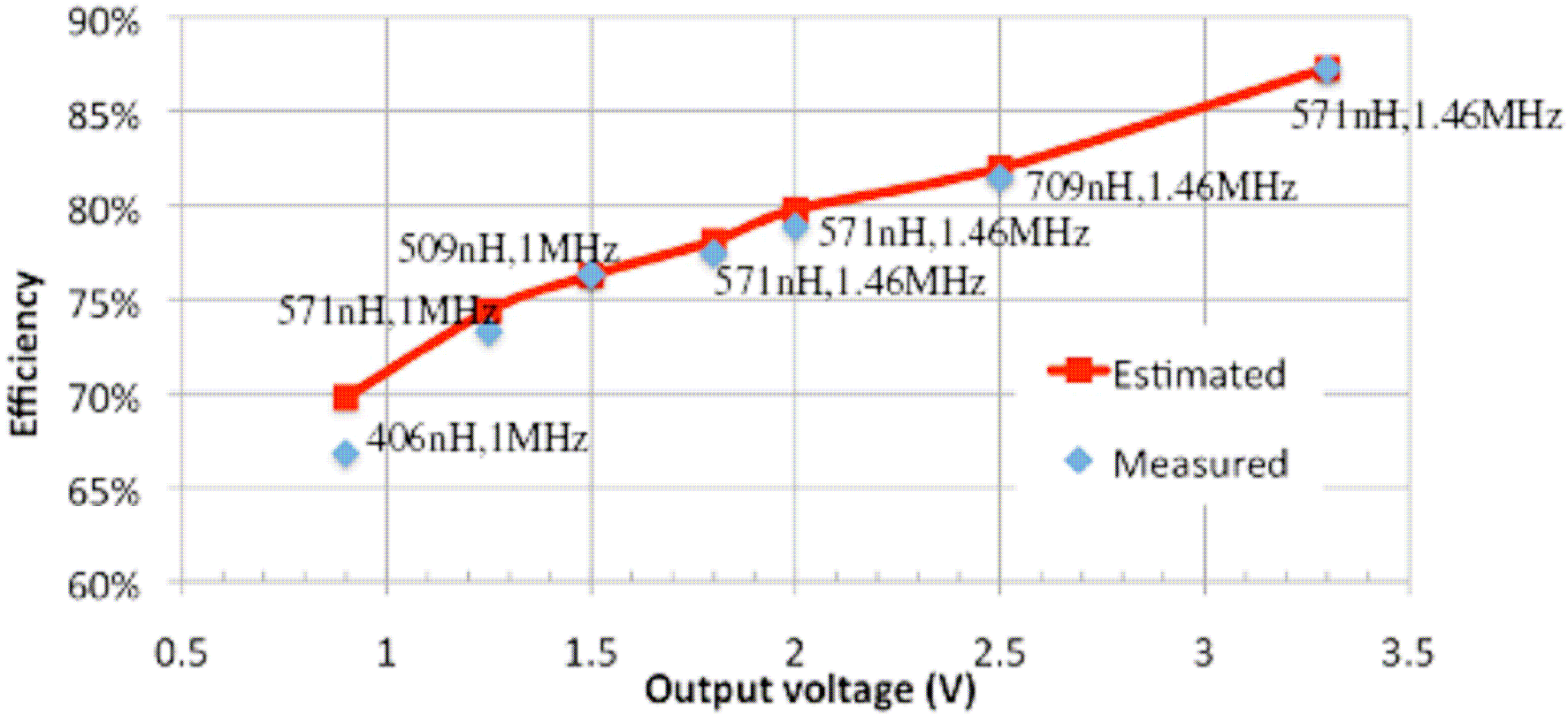
IHP 0.25µm ASIC V_{in}=7V, V_{out}=2.5V, I_{out}=1.3A, f_s=2MHz, L=538nH

Circuit on chip implementation



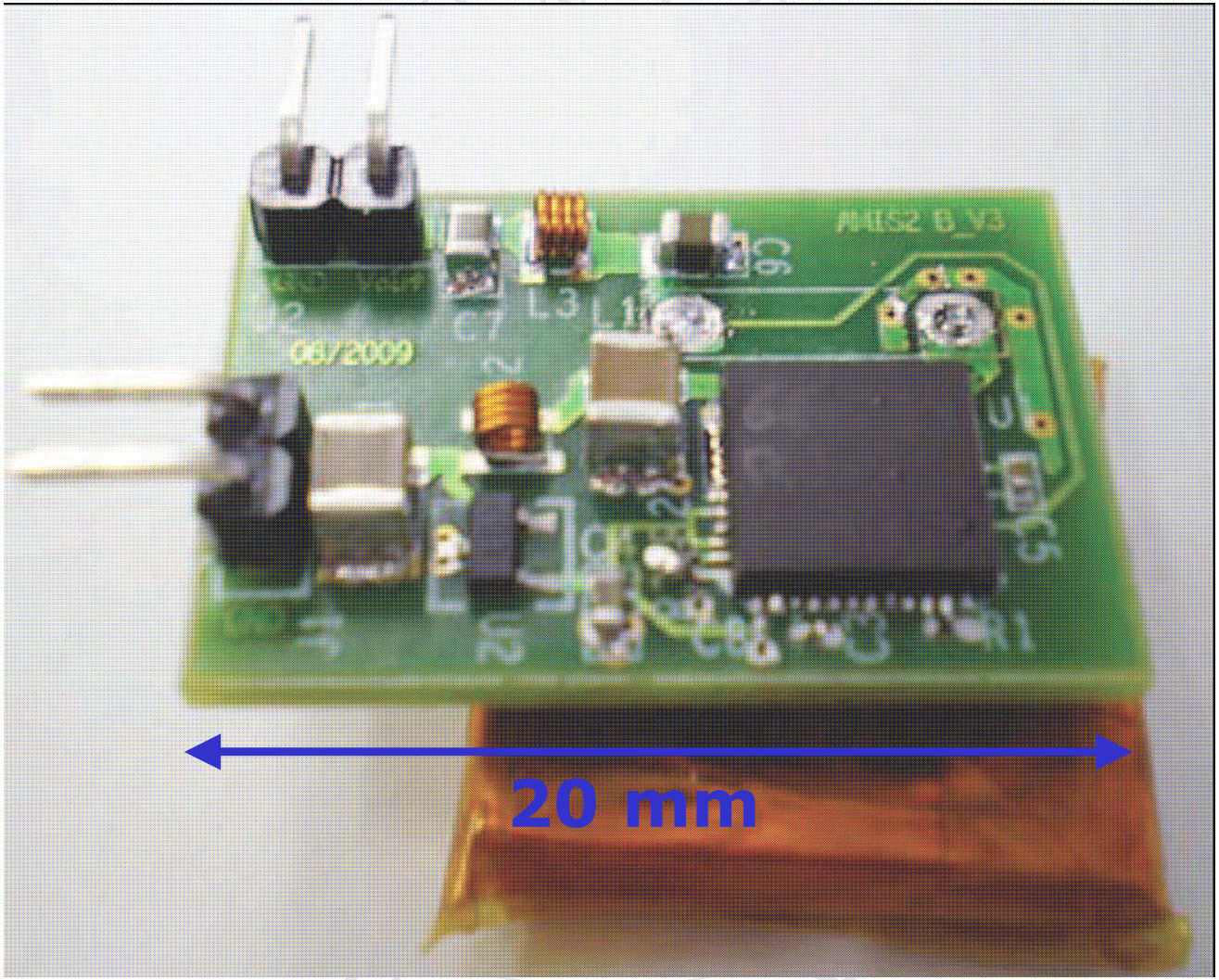
V_{in}=7V, I_{out}=2A, V_{out}=2.5V

Circuit on chip implementation



V_{in}=10V, I_{out}=1A

Circuit on chip implementation



Switched Capacitor Converters

The second conversion stage, to be implemented inside the read-out and communication chips, is implemented by means of switched capacitor converters (SCC).

These employ no inductance and present a typical voltage source characteristic, with equivalent output resistance depending on the switches´channel resistance, the capacitors' ESR and the commutation frequency.

Their conversion ratio is a function of the topology (number of capacitors and switches) and cannot be modified by control.

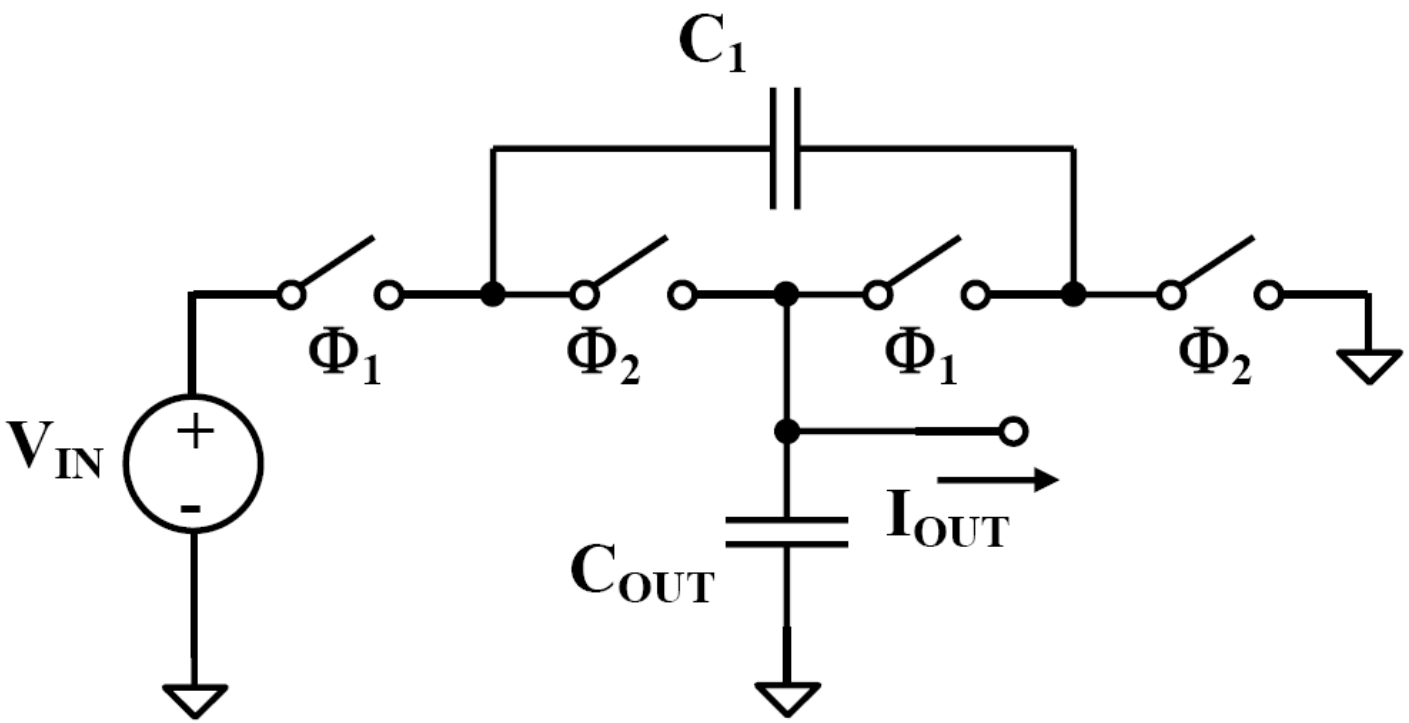
Switched Capacitor Converters

Table I – Basic SC converter specifications

Input voltage, V_{IN}	$2 \div 3$ V
Output voltage, V_{OUT}	$1 \div 2$ V
Maximum expected output current, I_{OUT}	1 A
Maximum output current variation	$\pm$ 100 mA

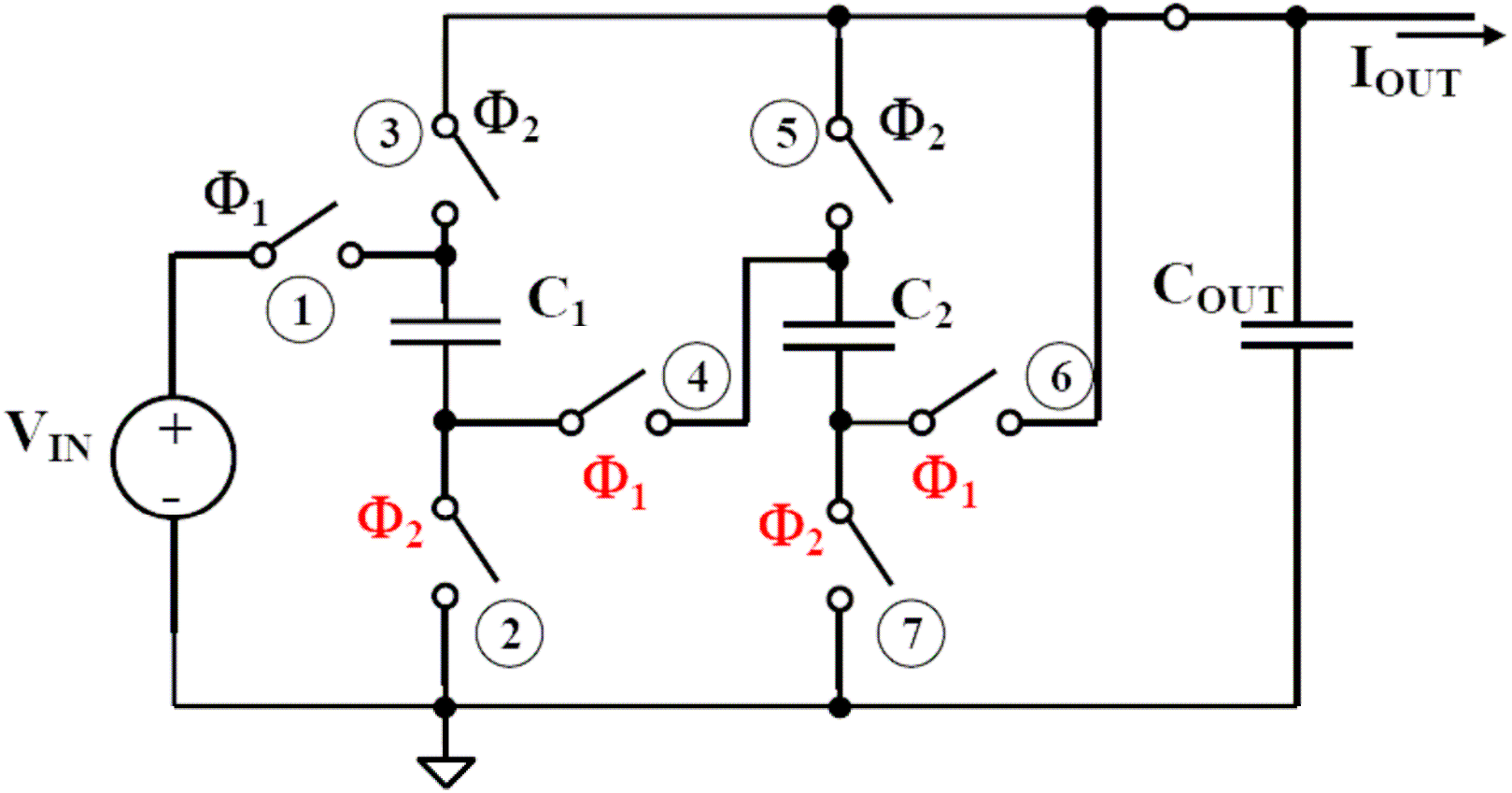
The required conversion ratio is between 0.67 and 0.33, including 0.5.

Switched Capacitor Converters



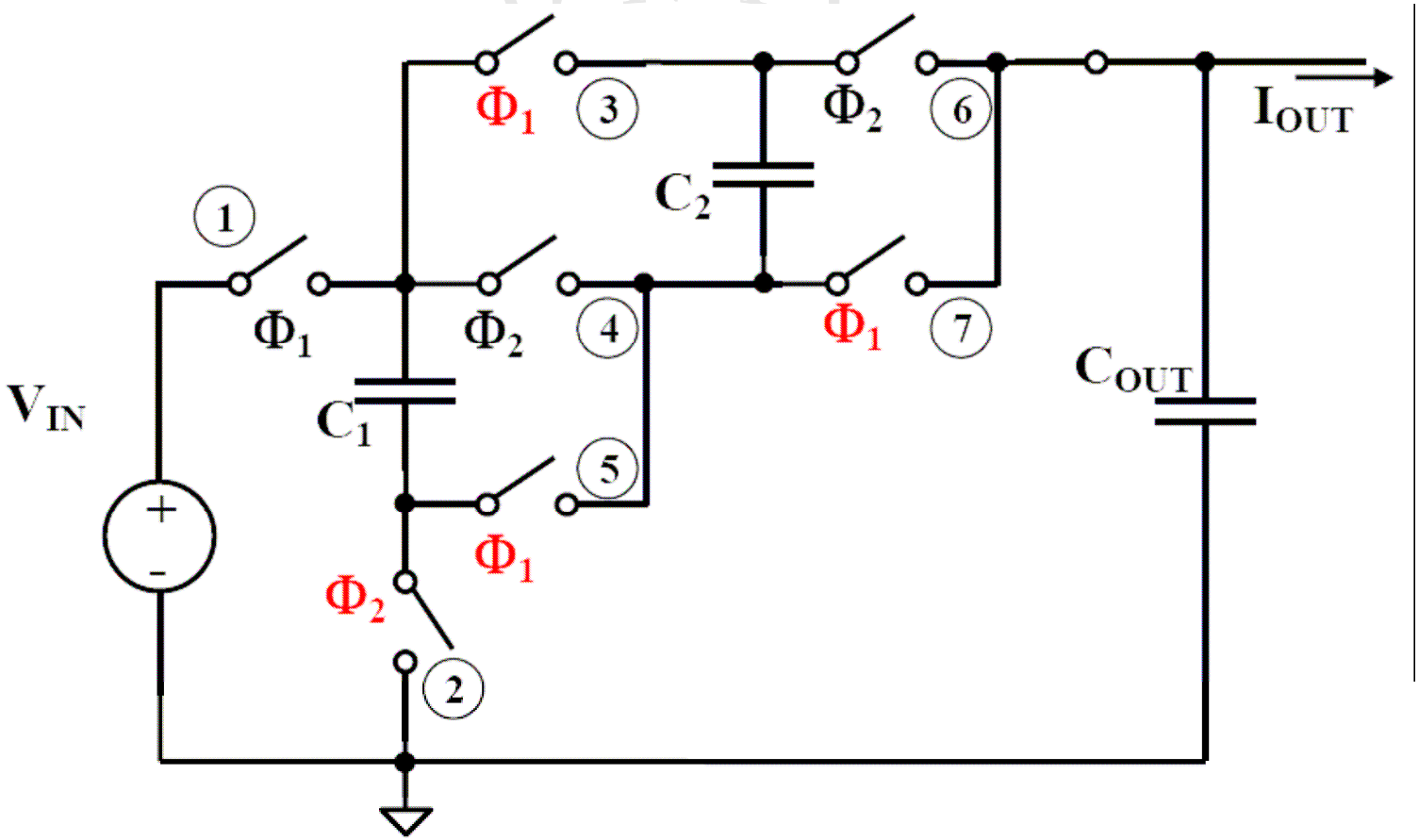
SCC topology for 0.5 conversion ratio

Switched Capacitor Converters



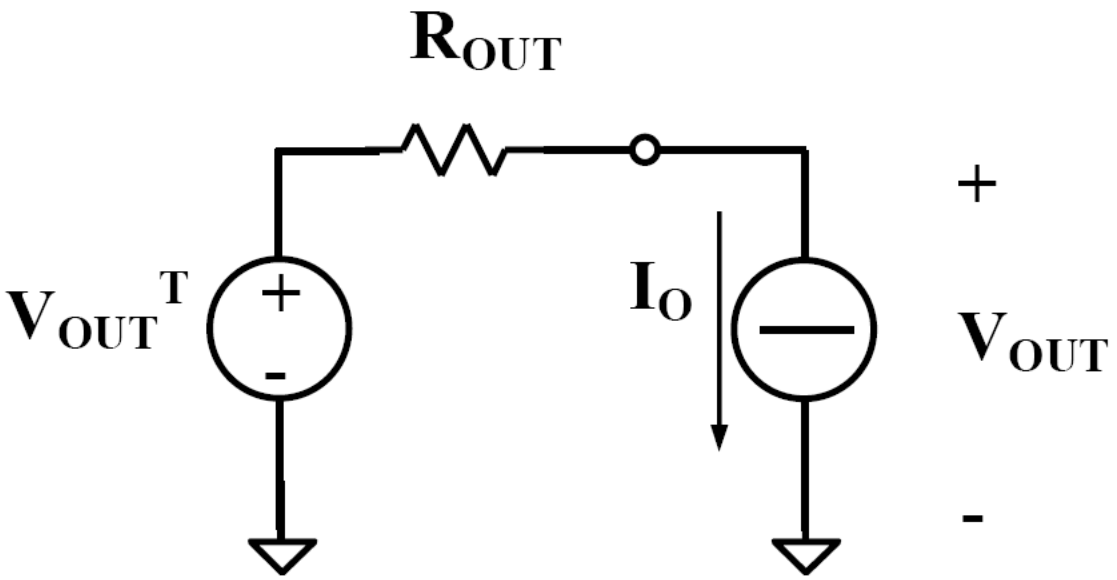
SCC topology for 0.33 conversion ratio

Switched Capacitor Converters



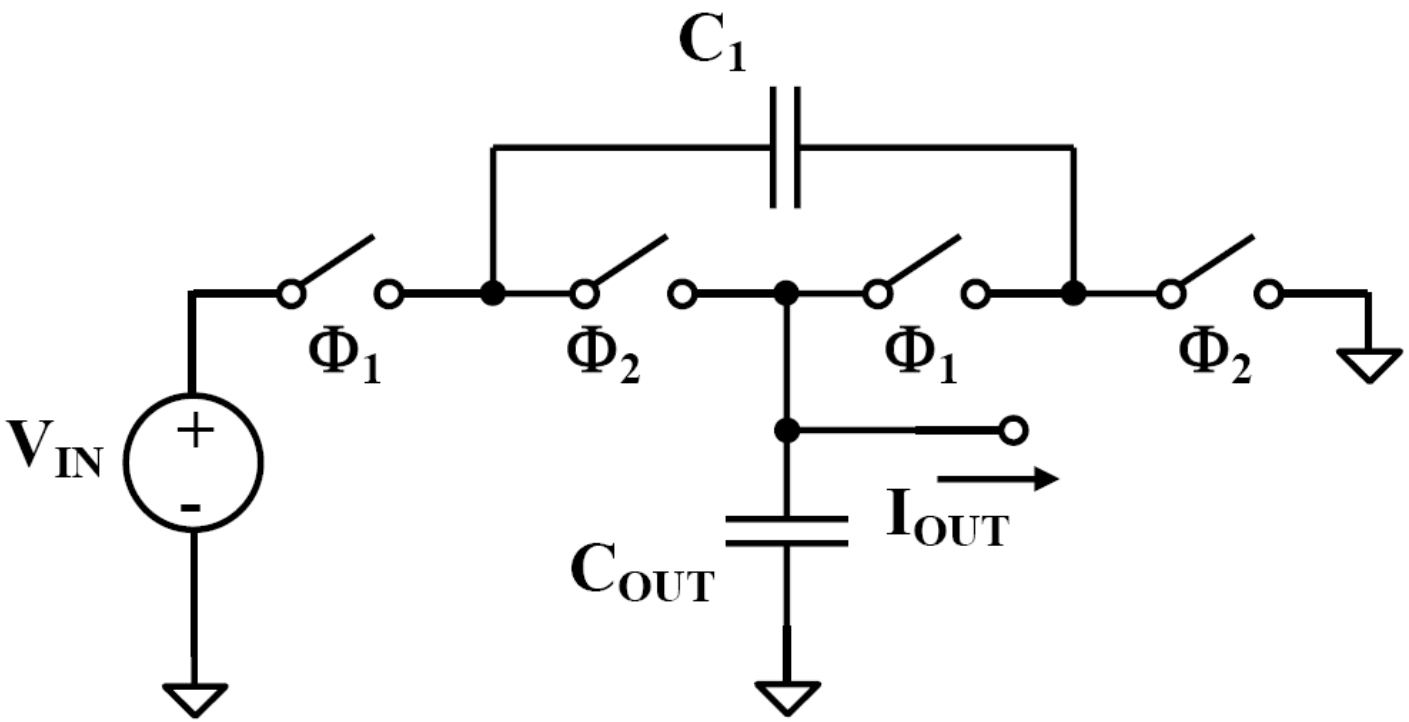
SCC topology for 0.67 conversion ratio

Switched Capacitor Converters



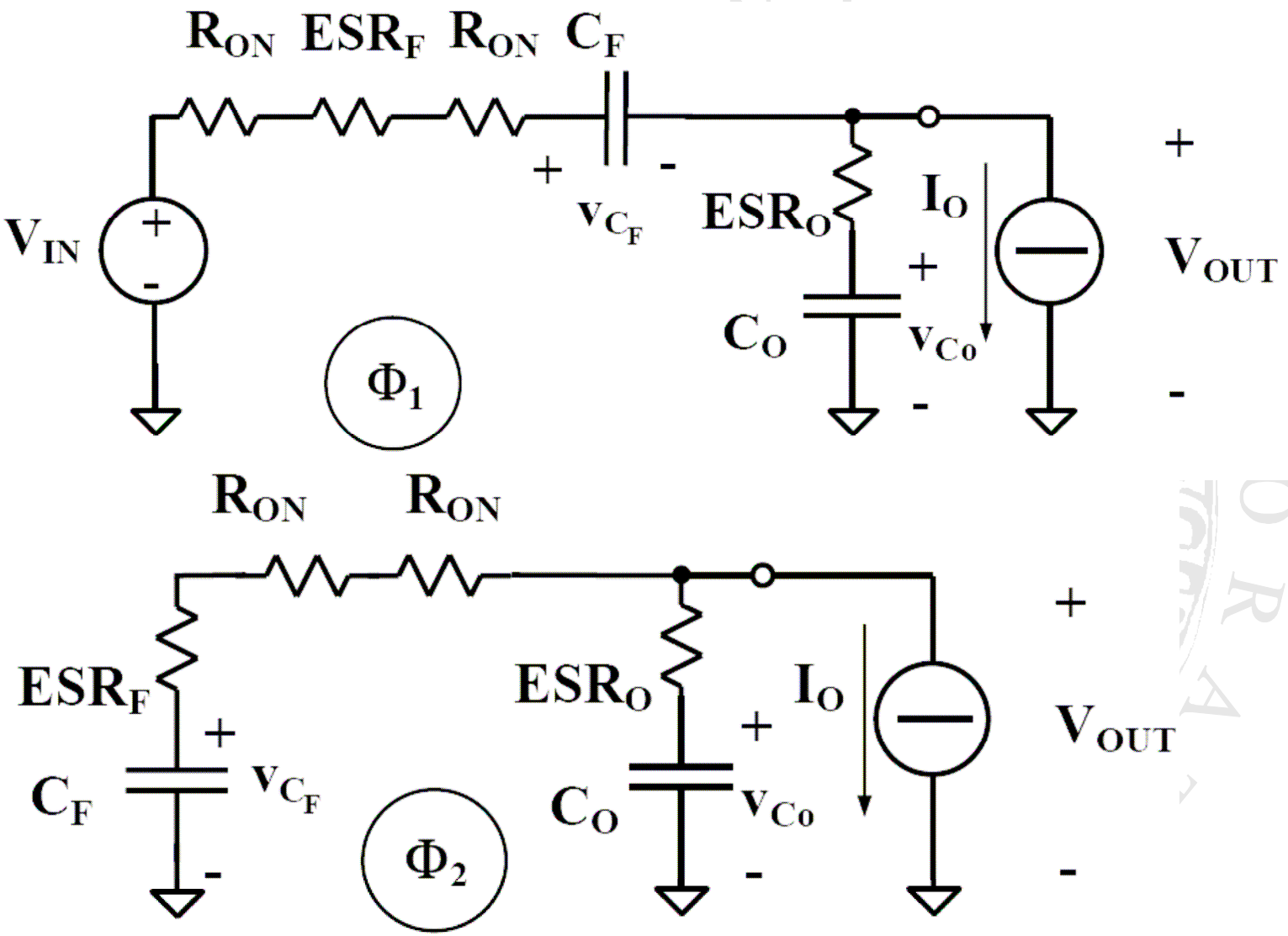
Simple equivalent model for a SSC converter. The measurable output voltage is affected by the equivalent output resistance.

SCCs with M=0.5: analysis



SSC topology for 0.5 conversion ratio

SCCs with M=0.5: analysis



SCCs with M=0.5: analysis

$$\begin{cases} \dot{v}_{C_F} = -\dfrac{ESR_O C_O}{R_T C_F} \cdot \dot{v}_{C_O} - \dfrac{v_{C_F}}{R_T C_F} - \dfrac{v_{C_O}}{R_T C_F} + \dfrac{V_{IN}}{R_T C_F} \\ \dot{v}_{C_O} = -\dfrac{ESR_O}{R_T} \cdot \dot{v}_{C_O} - \dfrac{v_{C_F}}{R_T C_O} - \dfrac{v_{C_O}}{R_T C_O} + \dfrac{V_{IN}}{R_T C_O} - \dfrac{I_O}{C_O} \end{cases}$$

$$R_T = 2R_{ON} + ESR_F$$

Differential equations for phase 1

SCCs with M=0.5: analysis

Solving the differential equations allows to determine V_{out} as a function of I_{out} and, consequently, R_{out}:

$$R_{OUT} = R_T\left(1+\left(\frac{\lambda}{1+\lambda}\right)^2(1+\alpha)\left(\left(\frac{T_C}{4\tau}\right)coth\left(\frac{T_C}{4\tau}\right)-1\right)\right)$$

$$\lambda = C_O/C_F$$

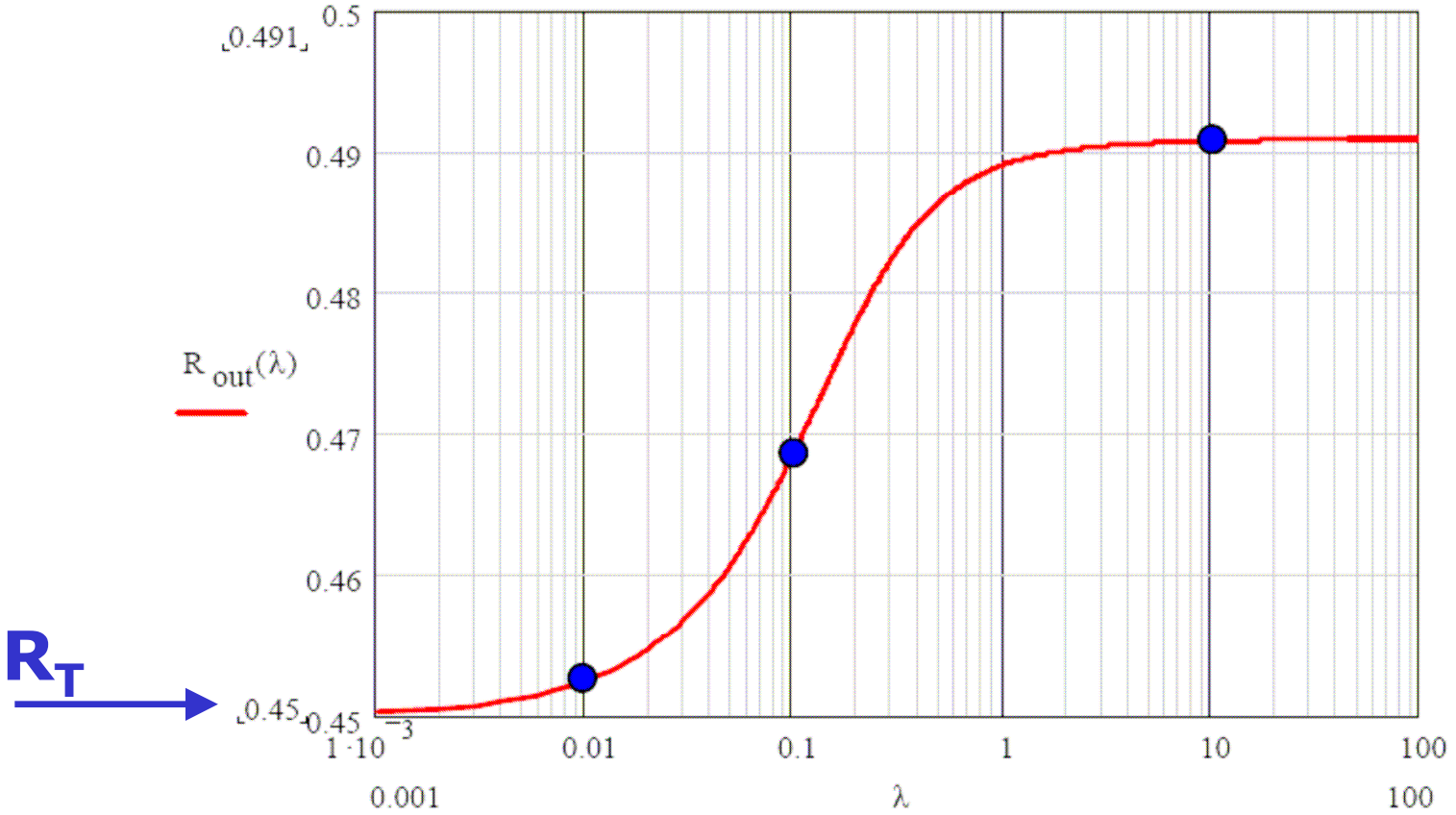
$$\alpha = ESR_O/R_T \qquad \tau = \frac{(1+\alpha)R_T C_O C_F}{C_O + C_F} = \frac{(1+\alpha)\tau_O \tau_F}{\tau_O + \tau_F} = \frac{1+\alpha}{1+\lambda}\tau_O$$

SCCs with M=0.5: analysis

TABLE II - CIRCUIT PARAMETERS

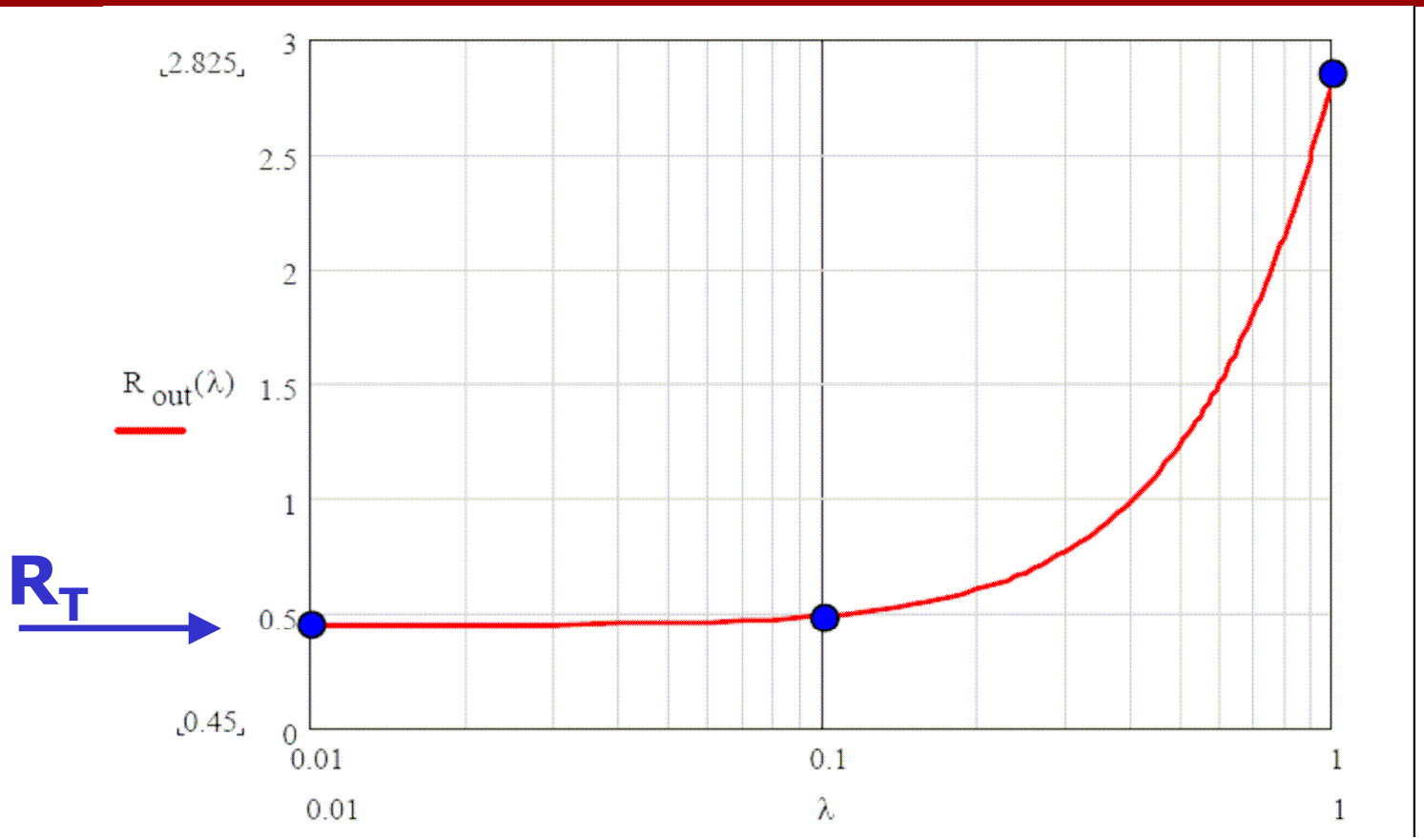
Input voltage	3	V
Output current	100	mA
Clock frequency	500	kHz
Flying capacitor, C_F	2	µF
Output capacitor, C_O	100	nF
Capacitor series resistance	50	mΩ
Switch on state resistance, R_{ON}	200	mΩ

SCCs with M=0.5: analysis



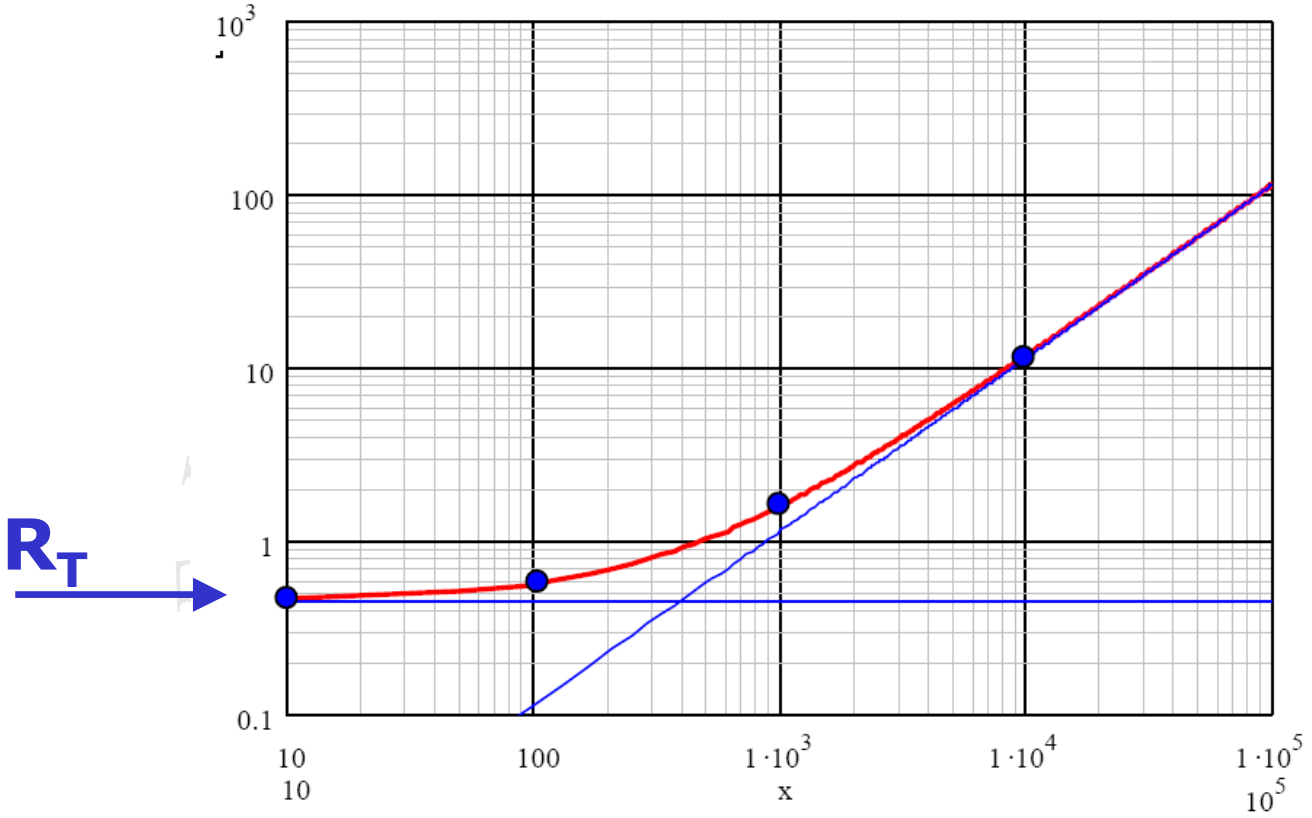
***D* = 0.5, F_C = 0.5 *MHz*: output resistance as a function of the capacitor ratio, λ.**
C_F = 2μF, variable C_O.

SCCs with M=0.5: analysis



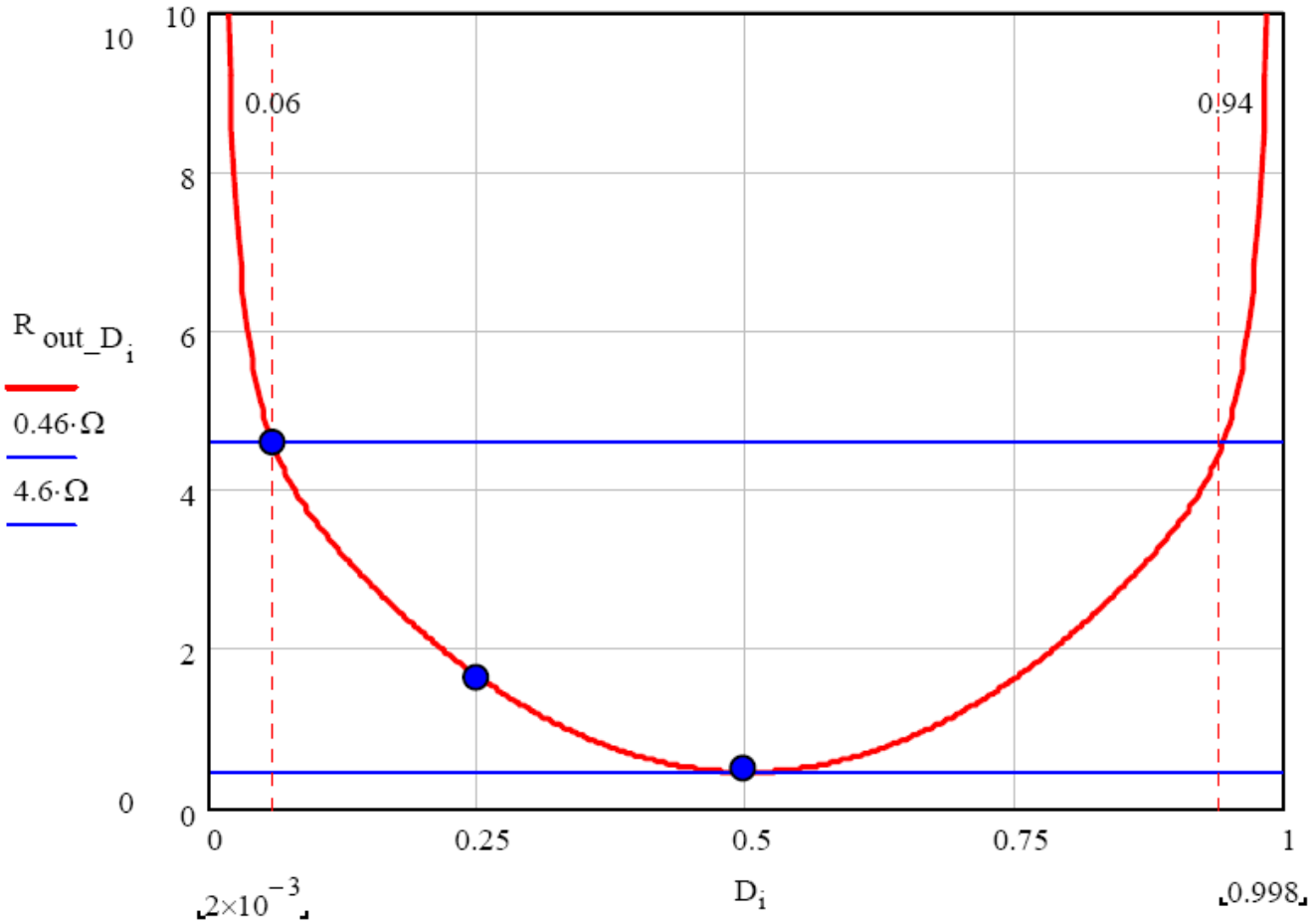
***D* = 0.5, F_C = 0.5 *MHz*: output resistance as a function of the capacitor ratio, λ.**
C_O = 0.1μF, variable C_F.

SCCs with M=0.5: analysis



D = 0.5, λ = 0.05, C_F = 2μF*: output resistance as a function of the clock period over circuit time constant ratio, *x

SCCs with M=0.5: analysis



***x = 0.024, λ = 0.05*: output resistance as a function of phase clock duty-cycle.**

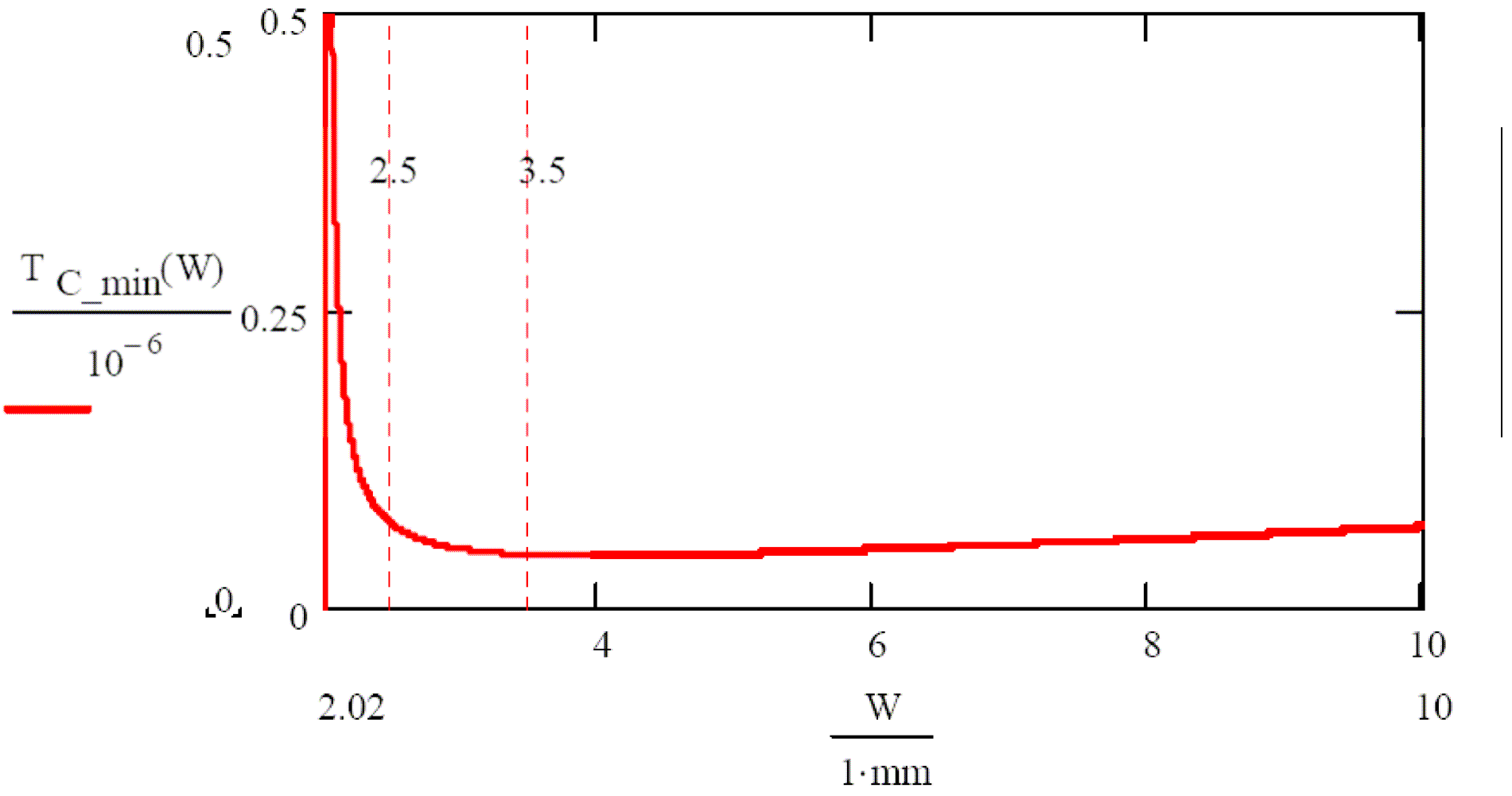
SCCs with M=0.5: design

For a given set of specifications, defining output power, output current, desired efficiency, the equation below poses a constraint between switch width W and clock period T_C.

$$\left(\frac{2r_{ON}}{W}+ESR_F\right)\cdot I_O^2+\frac{4c_{gs}\cdot W}{T_C}\cdot V_{GG}^2\le P_{loss\_total}$$

The equation is based on the assumption that the output resistance is very close to its *limit value,* R_T.

SCCs with M=0.5: design



SCCs with M=0.5: design

Considering the given specifications, we see that, for a solution to exist, the switch width must be, at least, 2 mm.

The plot shows that increasing the switch width too much above 3.5 mm, gives less and less advantage as the clock period tends to increase again.

Considering instead *W* = 2.5 mm, we can see that the maximum clock frequency is limited to about 14 MHz.

SCCs with M=0.5: design

However, the switching period upper limit is given by the maximum acceptable output resistance, i.e.

$$T_{C\_MAX} = \frac{4\tau(\lambda+1)^2}{\lambda^2(1+\alpha)} = \frac{4R_T C_O}{\lambda^2}(1+\lambda)$$

Finally, the output voltage ripple can be considered, to set a constraint on the total capacitance, i.e.

$$\Delta V_{Co} \cong \frac{I_o}{C_O + C_F}\frac{T_C}{2}$$

SCCs with M=0.5: design

The following design procedure can be outlined:

1. **select a suitable clock period, within the above specified limits;**
2. **determine the total capacitance required to keep the output voltage ripple below the desired limit;**
3. **impose a suitable λ value, i.e. 0.01;**
4. **determine C_O, C_F, R_{out};**
5. **repeat for lower period values until the limit for R_{out} is reached.**

Conclusions

Future High Energy Physics experiments at CERN require a complete re-design of the power distribution infrastructure.

Point of load converters have to be developed to bring voltage regulation as close as possible to the readout and communication electronics, inside the particle trajectory trackers.

This requires the identification of suitable integration technology and topology for the different conversion stages.

Conclusions

A buck converter ASIC has been developed as a first point of load voltage regulation stage, compatible with challenging radiation and magnetic field levels.

Radiation tolerance was obtained by technology selection combined to dedicated layout and circuit design practices, like redundancy and layout provisions (guard rings, shielding, etc. etc.).

Magnetic field tolerance forces the use of air-core inductors, in turn requiring high switching frequency.

Conclusions

To get the highest efficiency in the target application (V_{in} = 10-12 V, V_{out} = 1.8-3.3 V, I_{out} = 1-3 A) the design has been optimised for QSW mode, and a new control circuit, based on adaptive dead time management, has been successfully integrated.

The prototype yielded a reasonable measured efficiency, well matching the simulation model describing the different causes of energy loss.

Different designs, including the 2PBIVD topology, are currently under development.

Conclusions

Different Switched Capacitor Converters (SCCs) have been designed and simulated.

They will be integrated in the readout and control ASIC chips employed in the next generation sensors.

The achievable efficiency, the output voltage ripple and the overall volume occupation, determined by energy transfer capacitors (external), seem compatible with the volume budget.

Related papers

S. Orlandi, B. Allongue, G. Blanchot, S. Buso, F. Faccio, C. Fuentes, S. Michelis, G. Spiazzi, "Optimization of Shielded PCB Air-Core Toroids for High Efficiency DC-DC Converters", 2009 IEEE Energy Conversion Congress and Exposition, San Jose, California, USA, September 20-24, 2009, pp. 2073-2080.

S. Buso, G. Spiazzi, F. Faccio, S. Michelis, "Comparison of dc-dc converter topologies for future SLHC experiments", 2009 IEEE Energy Conversion Congress and Exposition, San Jose, California, USA, September 20-24, 2009, pp. 1775-1782.

C. Fuentes, B. Allongue, S. Buso, G. Blanchot, F. Faccio, S. Michelis, S. Orlandi, G. Spiazzi, "Power Distribution with Custom DC-DC Converters for SLHC Trackers", 2009 IEEE Nuclear Science Symposium Conference Record (NSS/MIC), Orlando, Florida, USA, October 25-31, 2009, pp. 1300-1305.

S. Michelis, B. Allongue, G. Blanchot, S. Buso, F. Faccio, C. Fuentes, A. Marchioro, S. Orlandi, S. Saggini, G. Spiazzi, M. Kayal, "An 8W-2MHz buck converter with adaptive dead time tolerant to radiation and high magnetic field", European Solid State Circuit Conference, ESSCIRC, Seville, Spain, September 13-17, 2010, pp. 438-441.

S. Orlandi, B. Allongue, G. Blanchot, S. Buso, F. Faccio, C. Fuentes Rojas, M. Kayal, S. Michelis, G. Spiazzi, "Optimization of shielded PCB air-core toroids for high efficiency dc-dc converters", IEEE Transactions on Power Electronics, in press.