Lesson 4

Implementation of Synchronous Frame Harmonic Control for High-Performance AC Power Supplies

Goal of the work

Investigation of selective control on output voltage harmonics.

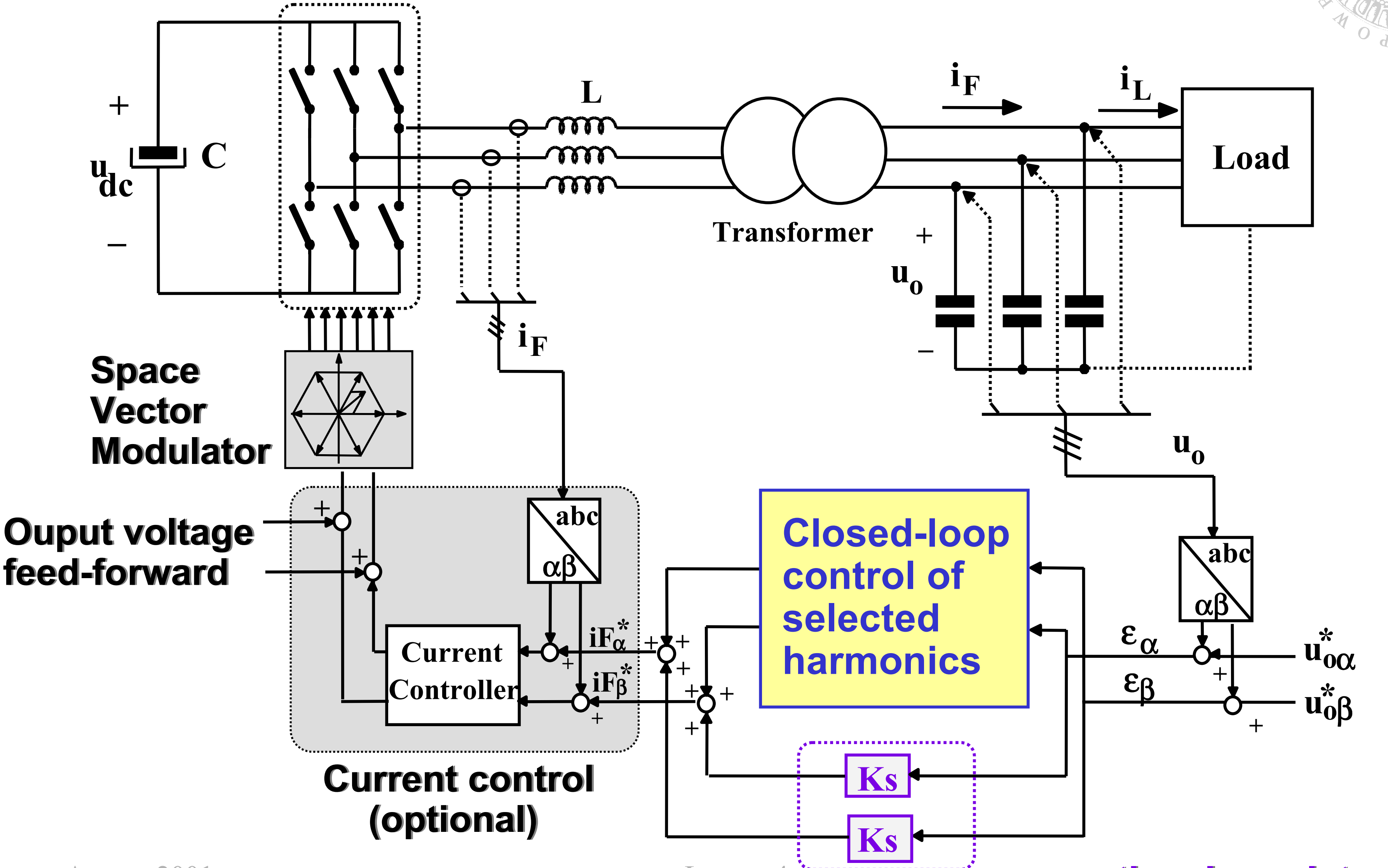
Motivations:

- **reduction of voltage distortion in AC Power Supplies (even with limited voltage loop bandwidth);**
- **refinements aimed at an efficient implementation in fixed-point DSP's (here tested on ADMC401 by Analog Devices).**

Presentation outline

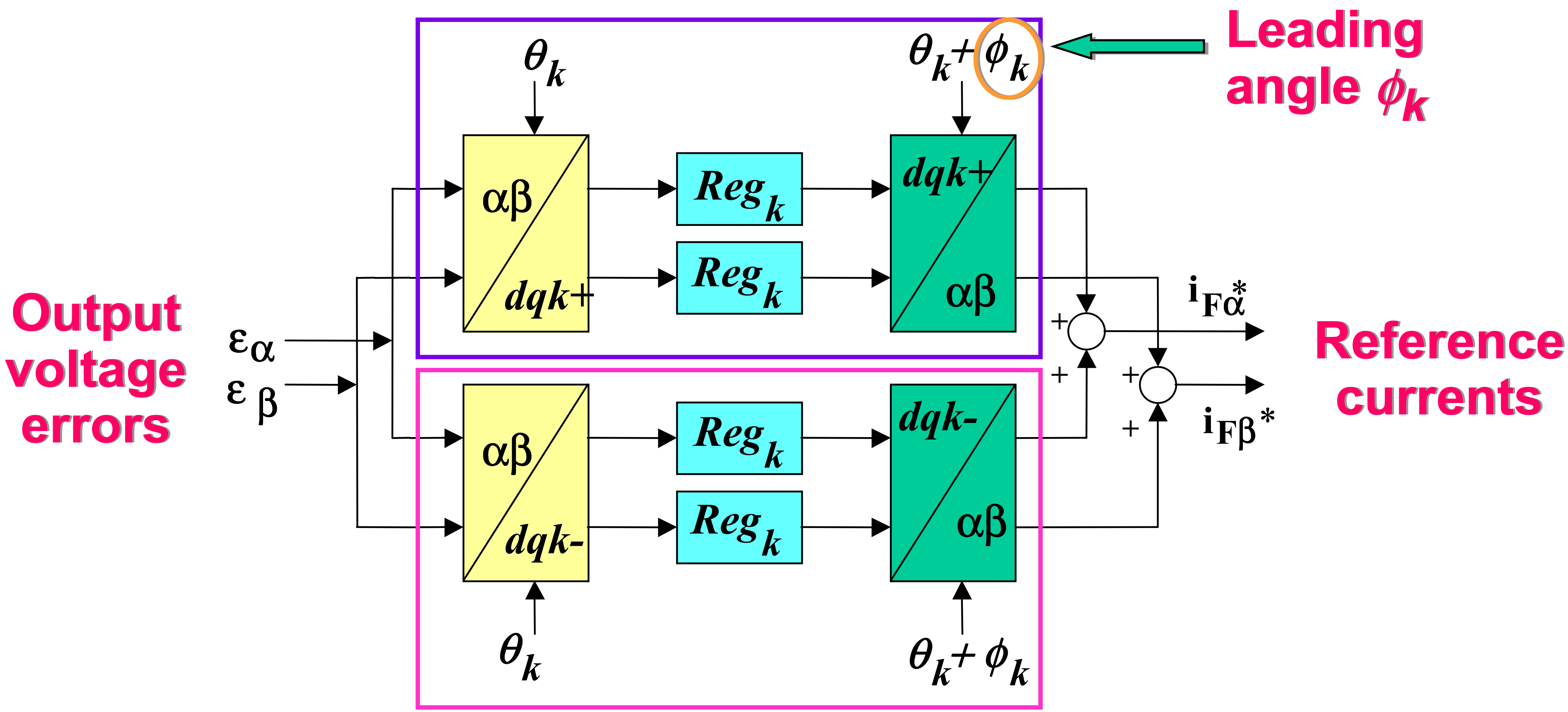
- Review of synchronous reference frame harmonic regulation
- Decomposition in three-layer control scheme
- A modified solution based on Discrete Fourier Transform
- Design guidelines for regulator parameters
- DSP implementation using ADMC401
- Experimental results

Synchronous frame harmonic control



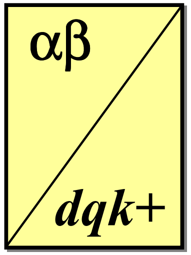
Basic scheme

Regulation of positive sequence k-th harmonic

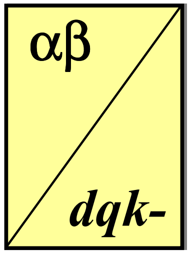


Regulation of negative sequence k-th harmonic

Basic scheme equations

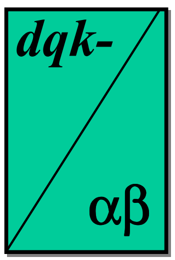


$$\begin{bmatrix} \varepsilon_{dk+} \\ \varepsilon_{qk+} \end{bmatrix} = \begin{bmatrix} \cos(k\omega_s t) & \sin(k\omega_s t) \\ -\sin(k\omega_s t) & \cos(k\omega_s t) \end{bmatrix} \begin{bmatrix} \varepsilon_{\alpha} \\ \varepsilon_{\beta} \end{bmatrix}$$



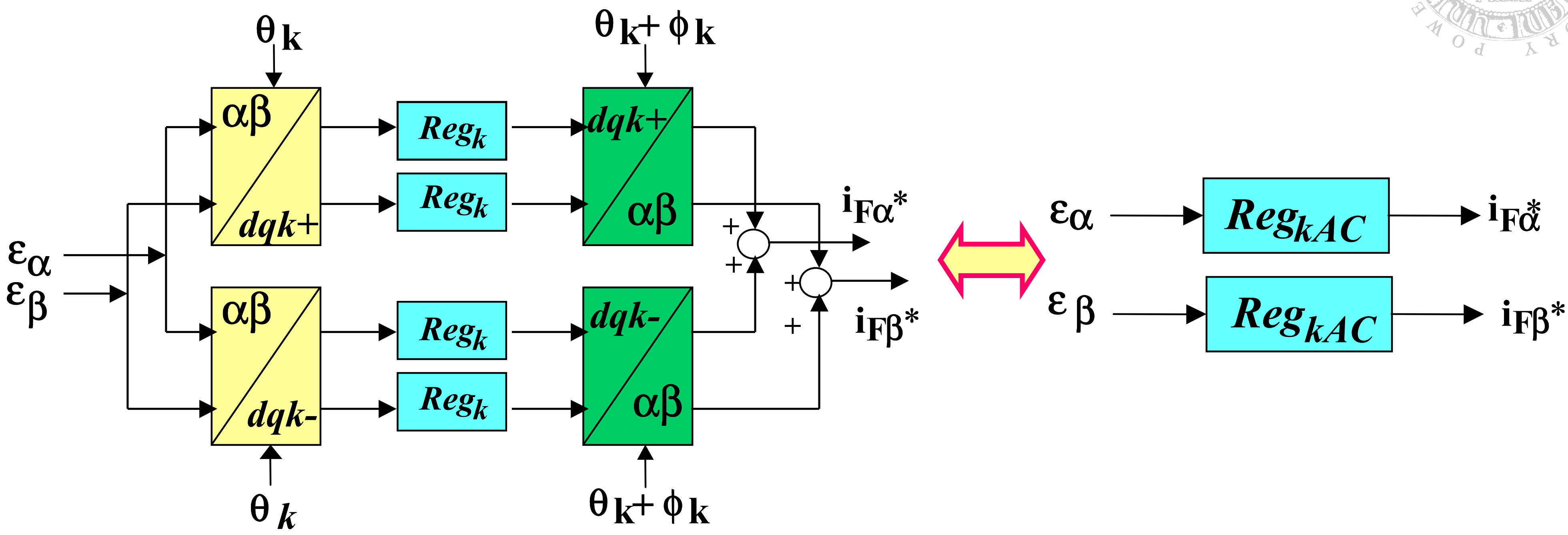
$$\begin{bmatrix} \varepsilon_{dk-} \\ \varepsilon_{qk-} \end{bmatrix} = \begin{bmatrix} \cos(k\omega_s t) & -\sin(k\omega_s t) \\ \sin(k\omega_s t) & \cos(k\omega_s t) \end{bmatrix} \begin{bmatrix} \varepsilon_{\alpha} \\ \varepsilon_{\beta} \end{bmatrix}$$

$$\begin{bmatrix} y_{\alpha k-} \\ y_{\beta k-} \end{bmatrix} = \begin{bmatrix} \cos(k\omega_s t + \phi_k) & \sin(k\omega_s t + \phi_k) \\ -\sin(k\omega_s t + \phi_k) & \cos(k\omega_s t + \phi_k) \end{bmatrix} \begin{bmatrix} y_{dk-} \\ y_{qk-} \end{bmatrix}$$



$$\begin{bmatrix} y_{\alpha k+} \\ y_{\beta k+} \end{bmatrix} = \begin{bmatrix} \cos(k\omega_s t + \phi_k) & -\sin(k\omega_s t + \phi_k) \\ \sin(k\omega_s t + \phi_k) & \cos(k\omega_s t + \phi_k) \end{bmatrix} \begin{bmatrix} y_{dk+} \\ y_{qk+} \end{bmatrix}$$

Equivalence with stationary frame control



Equivalence

$$
\begin{aligned}
Reg_{kAC}(s) = \cos\phi_k\left[Reg_k(s - jk\omega_s) + Reg_k(s + jk\omega_s)\right] + \\
+ j\sin\phi_k\left[Reg_k(s - jk\omega_s) - Reg_k(s + jk\omega_s)\right]
\end{aligned}
$$

Equivalence with stationary frame control

- If $Reg_k(s)$ is a integral regulator, the previous equivalence implies that $Reg_{kAC}(s)$ is a band-pass filter centered on the k^{th} harmonic frequency.
- This is true if and only if both direct and reverse sequence controllers are implemented.
- It is possible to implement synchronous regulators either in the dq rotating frame or in the $\alpha\beta$ stationary frame, with perfectly equivalent performance.

Equivalence with stationary frame control

- The leading angle ϕ_k can be used to compensate for internal delays, such as that of the current controller.
- In practice, the current reference is phase shifted to compensate for the current controller delay.
- In the stationary frame implementation, based on band-pass filters, this may or may not have a possible equivalent (depending on the regulator structure).

Three-layer decomposition

AC Power Supplies requirements

- Fast transient response with limited overshoot under load changes;
- Possibly fast regulation of output voltage fundamental harmonic component;
- For distorting loads with slowly-varying harmonics, harmonic control in some fundamental cycles (decoupling between different controllers is needed!).

Three-layer decomposition

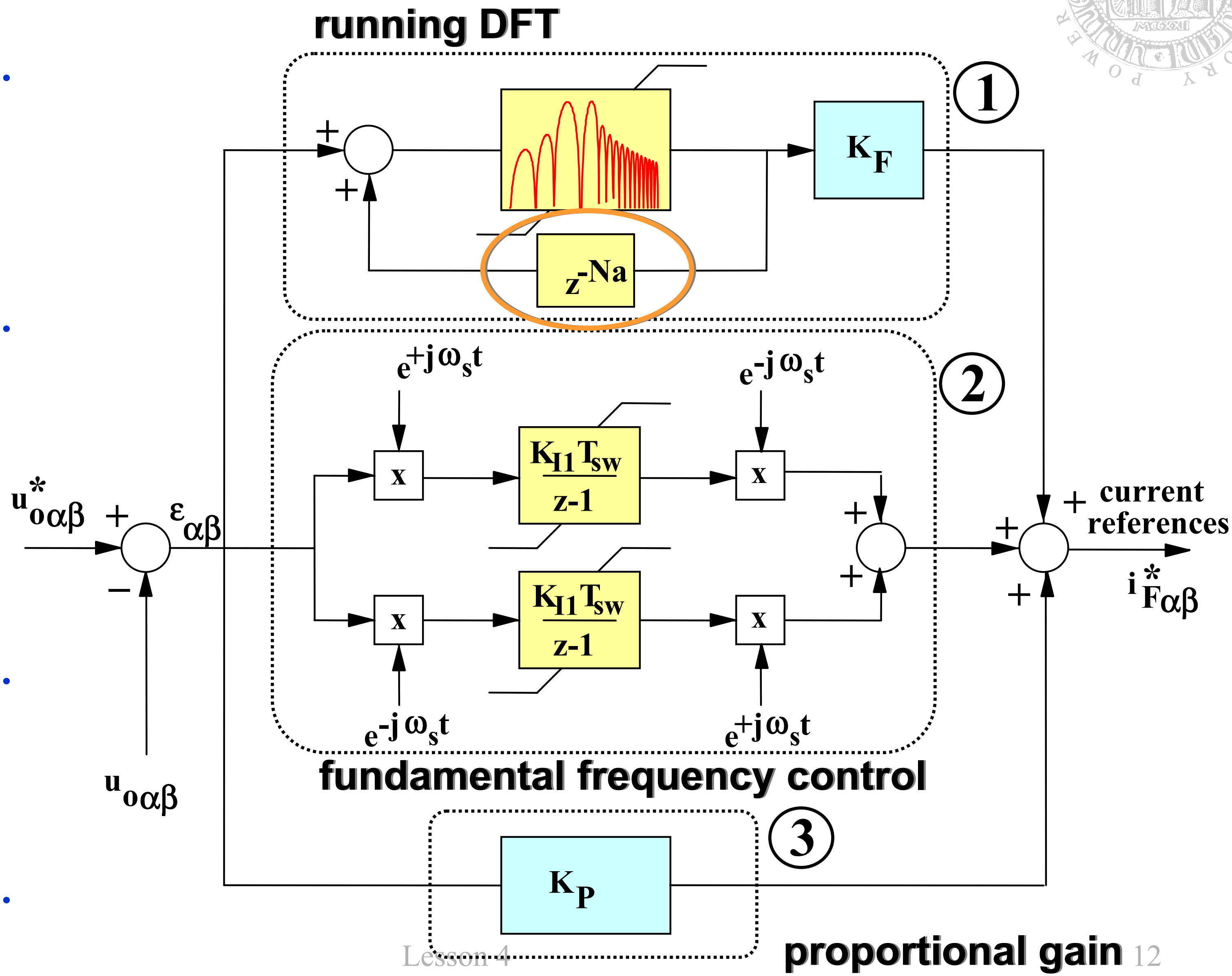
- The previous requirements suggest a decomposition of the control system in three layers:
  - reference tracking control (for a quick dynamic response) ⇒ loop bandwidth;
  - fundamental component control ⇒ high loop gain at the fundamental frequency, with low selectivity;
  - harmonics control ⇒ high loop gain at each harmonic frequency with high selectivity.

Three-Layer Decomposition

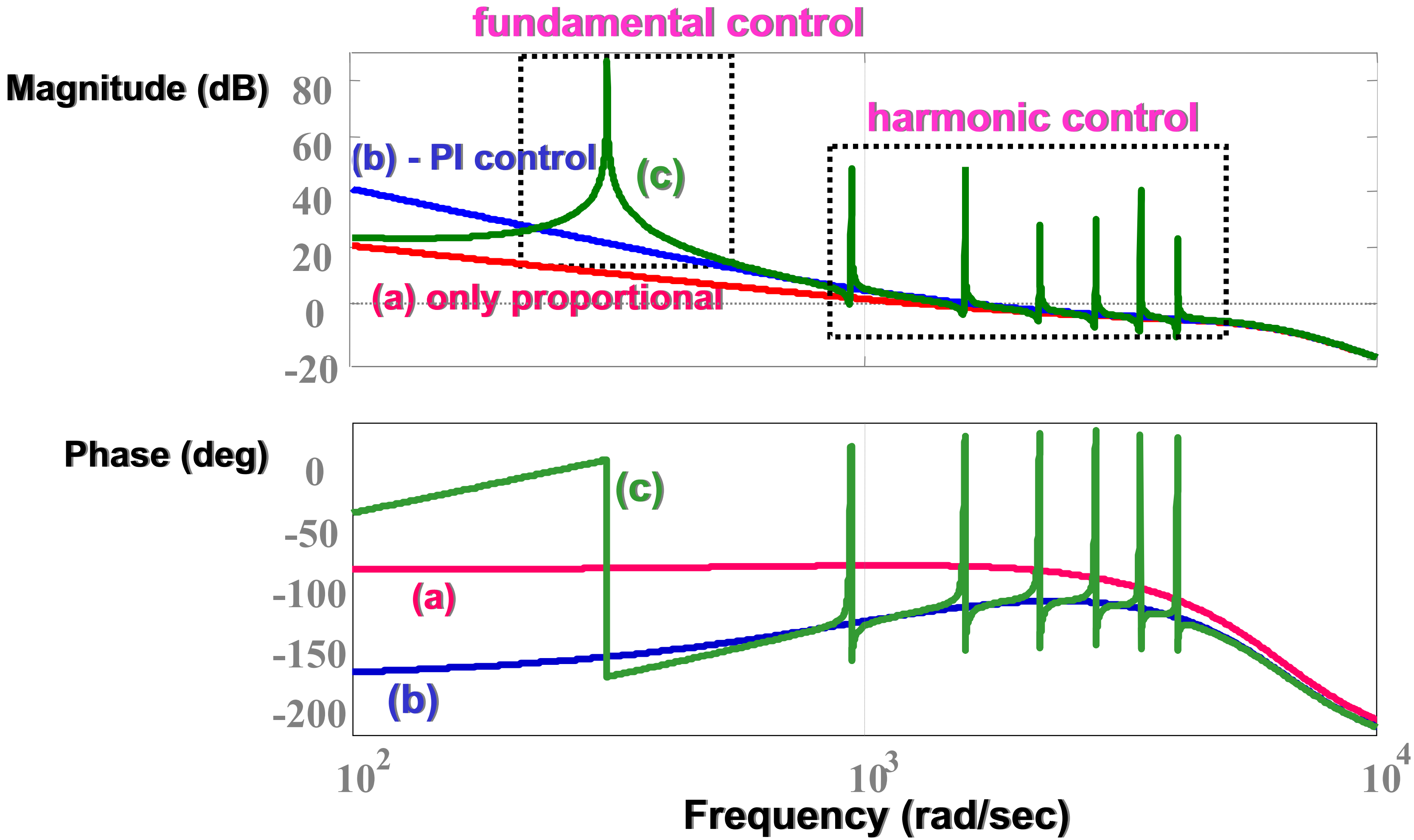
Harmonics Control

Fundamental Component Control

Tracking Control



Bode diagram of open loop gain



(a) only proportional gain (b) PI control

(c) integral rotating-frame regulators

Notes

- In principle, harmonics could be controlled by integral, rotating frame regulators.
- This solution is cumbersome, requiring a large number of dq transformations.
- The AC equivalent of the integral controller is a high selectivity band-pass filter. This is difficult to implement because of fixed point arithmetic.
- Even if no stability problems can be generated, the selectivity is strongly limited by rounding errors affecting the filter coefficients.

Harmonic control

F_h- pass-band filter with unity gain and zero phase at harmonic h, with good selectivity

$$\operatorname{Re} g_{hAC}(s) = \sum_{h \in N_h} \frac{2K_{Ih}\, s}{s^2 + (h\omega_s)^2} = K_F \sum_{h \in N_h} \frac{F_h}{1 - F_h} \approx K_F \frac{\sum_{h \in N_h} F_h}{1 - \sum_{h \in N_h} F_h}$$

K_F is defined as follows:

$$K_F = \frac{K_{Ih}}{\xi_h h \omega_s}$$

K_F is constant provided K_{Ih} are equal to $h \cdot K_I$

Harmonic control

The above approximation is well verified by several types of band-pass filters. A good choice, which offers significant implementation advantages, is represented by FIR filters based on DFT such as:

$$F_{dh}(z) = \frac{2}{N}\sum_{i=0}^{N-1}\cos\left[\frac{2\pi}{N}hi\right]z^{-i}$$

For a single harmonic frequency

Harmonic control

$$F_{dh}(z) = \frac{2}{N}\sum_{i=0}^{N-1}\cos\left[\frac{2\pi}{N}hi\right]z^{-i}$$

- This equation is based on the expression of the h-th harmonic component of a given input signal's DFT to derive a filter (running DFT).
- The structure is that of a typical FIR filter (linear combination of delays).
- From this standpoint $N \cdot T_s$ (T_s is the sampling period) does not necessarily represent the period of the input signal, which can be even non-periodic.

Harmonic control

$$F_{dh}(z) = \frac{2}{N}\sum_{i=0}^{N-1}\cos\left[\frac{2\pi}{N}hi\right]z^{-i}$$

FIR filter transfer function

Computing this equation in the time-domain gives:

$$y_h(k) = \frac{2}{N}\sum_{i=0}^{N-1}\cos\left[\frac{2\pi}{N}hi\right]x(k-i)$$

coefficients are not time dependent!

$y_h(k)$ is a sinusoidal signal that represents the projection of the input signal $x(k)$ upon the cosine base function of order h.

Harmonic control

Comparison with DFT:

$$y_h(k) = \frac{2}{N}\sum_{i=0}^{N-1}\cos\left[\frac{2\pi}{N}hi\right]x(k-i)$$

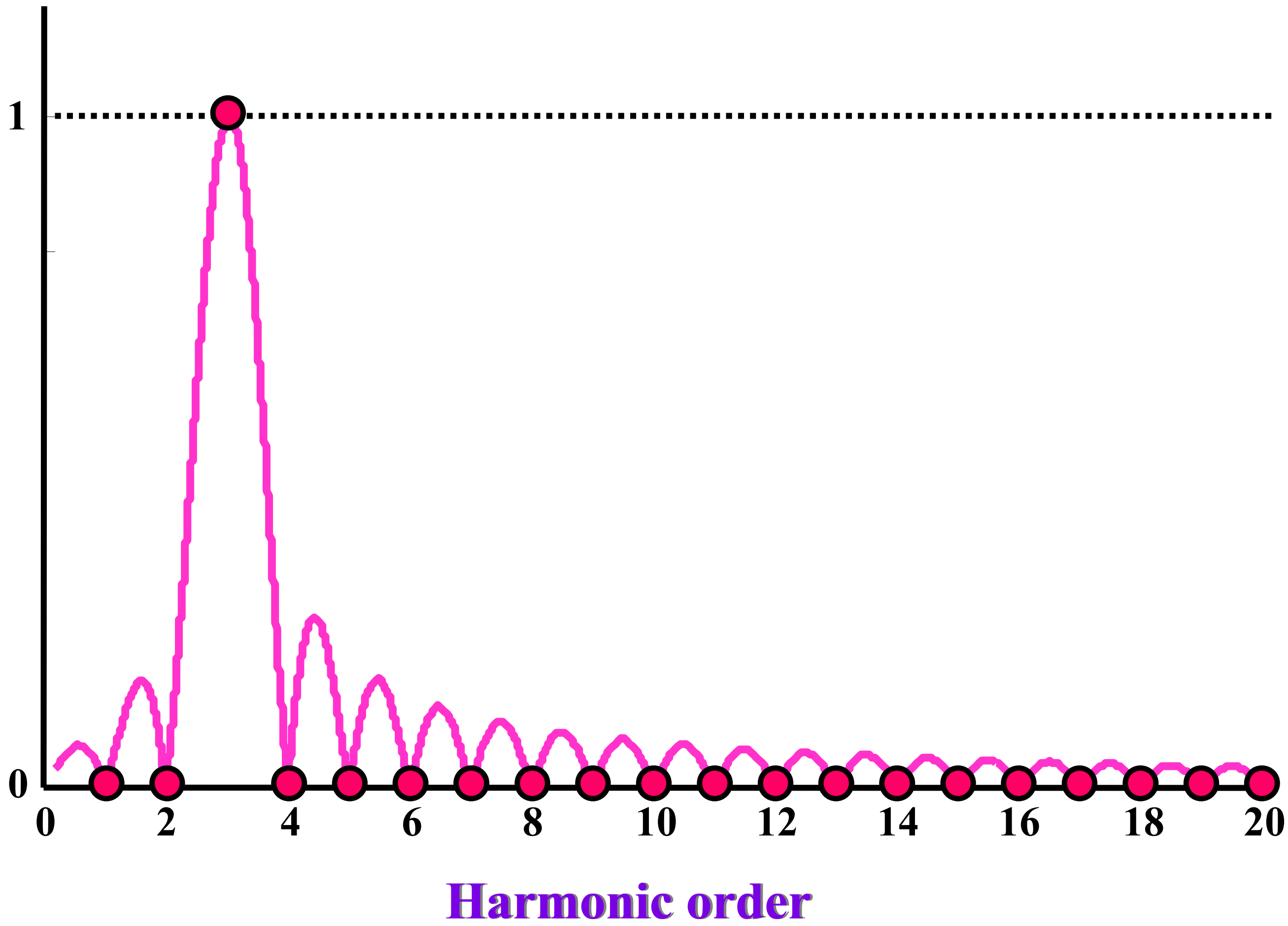
FIR filter

$$X_N(h) = \sum_{k=0}^{N-1}\cos\left[\frac{2\pi}{N}hk\right]x(k)$$

h^{th} order cosine component in the DFT of signal x(k)

k is the time index, so in the DFT coefficients are time dependent. The structure of the two algorithms is exactly the same.

Harmonic control



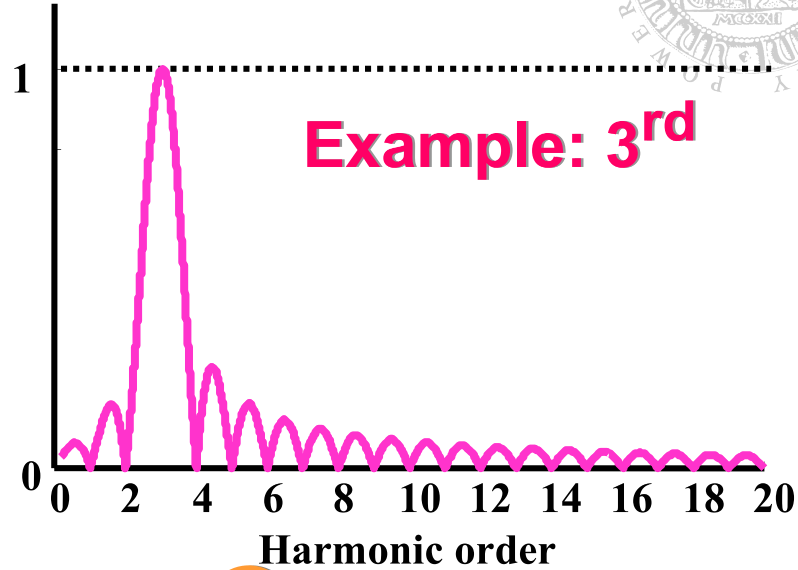
- Sampled frequency response, as seen by signals with period $N \cdot T_s/h$.

Frequency response of function $F_{dh}(z)$ for $h = 3$.

Harmonic control

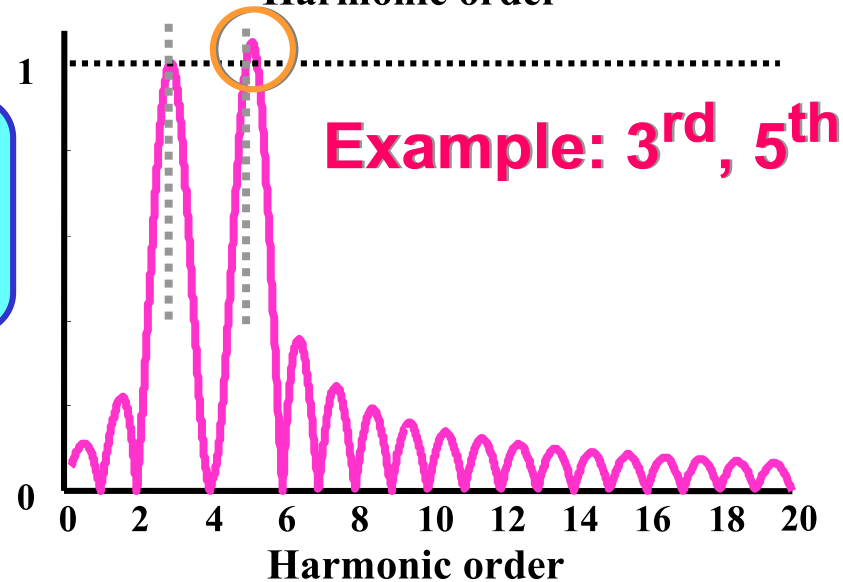
For a single harmonic

$$F_{dh}(z)=\frac{2}{N}\sum_{i=0}^{N-1}\cos\left[\frac{2\pi}{N}hi\right]z^{-i}$$



For multiple frequencies

$$\sum_{h\in N_h}F_{dh}(z)=\frac{2}{N}\sum_{i=0}^{N-1}\left(\sum_{h\in N_k}\cos\left[\frac{2\pi}{N}hi\right]\right)z^{-i}$$



No additional calculations for more harmonics

Harmonic control

$$\sum_{h\in N_h} F_{dh}(z) = \frac{2}{N}\sum_{i=0}^{N-1}\left(\sum_{h\in N_k}\cos\left[\frac{2\pi}{N}hi\right]\right)z^{-i}$$

- The coefficient for the i-th term can be computed off-line according to:

$$\sum_{h\in N_k}\cos\left[\frac{2\pi}{N}hi\right]$$

- The control complexity does not depend on the number of harmonic components taken into account.

Design Criteria

Fundamental frequency control

Proportional terms and fundamental frequency control are based on specified bandwidth and phase margin:

Equivalence with PI

$$K_{I1} = K_{Ic} \frac{\omega_c^2 - \omega_s^2}{2\,\omega_c^2}$$

K_{Ic} is the integral gain of a conventionally designed PI regulator.

Harmonic control

- **Amplification of frequencies close to the harmonics is an undesired effect of the filter superposition.**
- **Introduction of the leading angle ϕ_k is possible by means of positive feedback, provided that the angle is proportional to the harmonic frequency.**
- **Internal delays can be compensated.**

$$\sum_{h \in N_h} F_{dh}(z) = \frac{2}{N} \sum_{i=0}^{N-1} \left(\sum_{k \in N_k} \cos\left[\frac{2\pi}{N} k (i + N_a) \right] \right) z^{-i}$$

Design Criteria

Harmonic control

Specification on the response time (n_{pk})

$$K_{lk} = \frac{2.2}{n_{pk} T_S}$$

n_{pk} is the desired number of fundamental cycles for the dynamic response. It must be high enough to provide de-coupling with the fundamental frequency control. The equation is derived by approximated relations between gain and settling time of 2nd order band-pass filters.

Design Criteria

Harmonic control

gain of DFT filters

$$K_F \approx \frac{K_{Ik}}{0.32\,\omega_s}$$

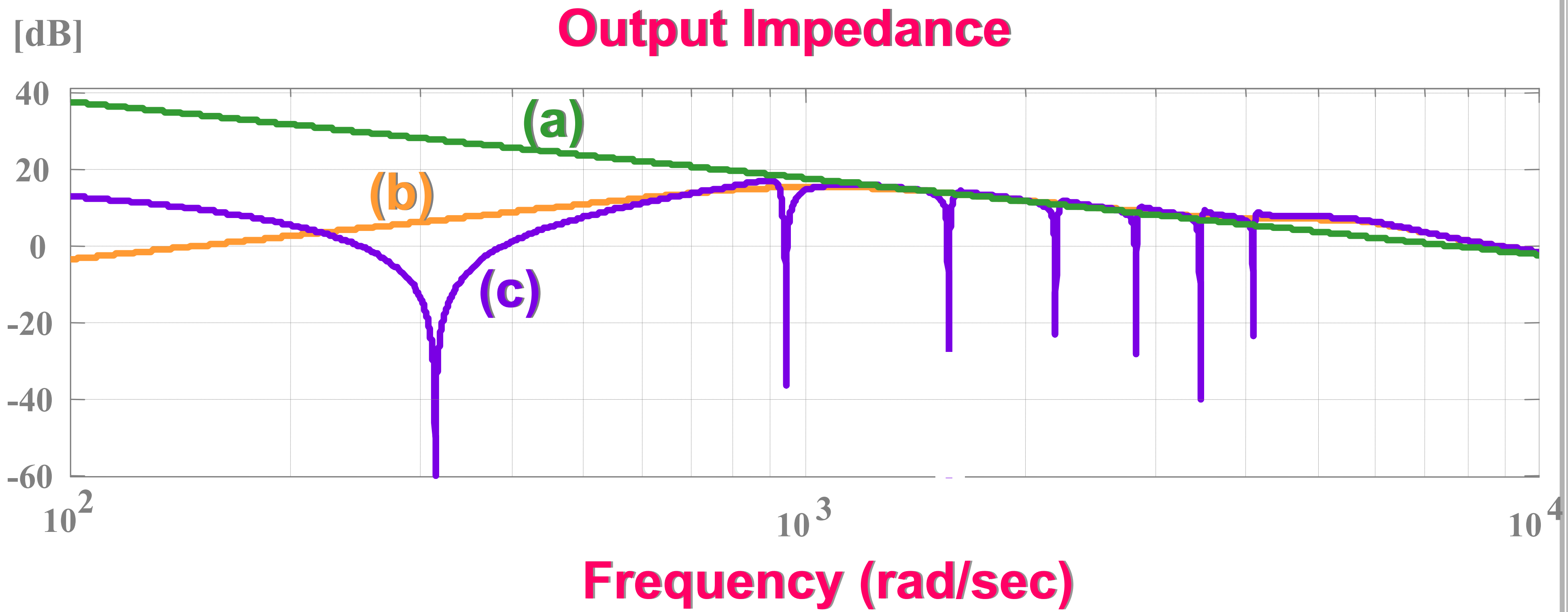
This relation is based on the approximation of the single DFT filter with a conventional second order band-pass filter.
By trial and errors the 0.32 coefficient can be determined as the one minimizing the “distance” between the two frequency responses.

Closed-loop Output Impedance

(a) only proportional gain

(b) PI control

(c) integral rotating-frame regulators

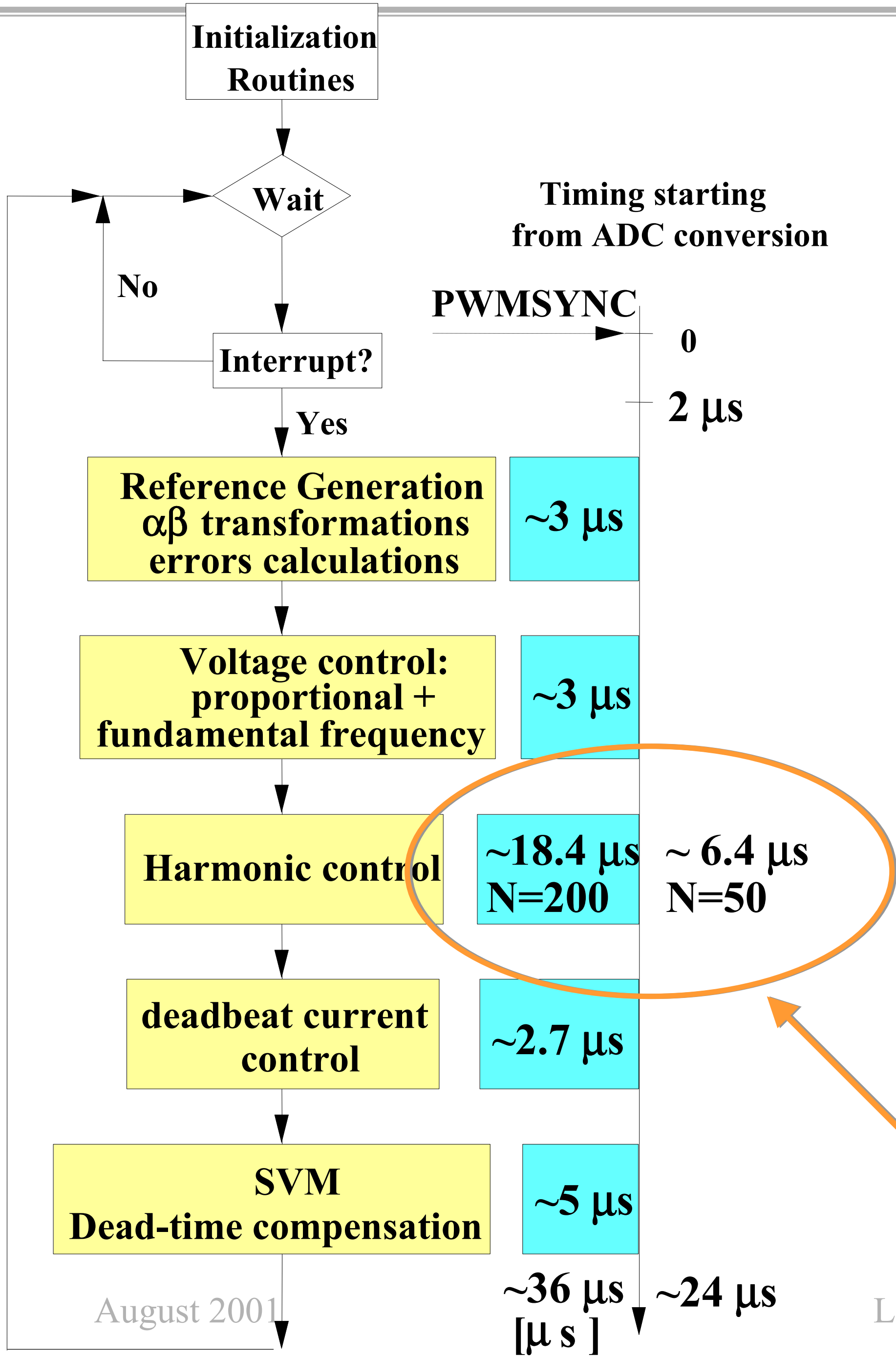


DSP Implementation

Main features of DSP-based controller ADMC401:

- 16-bit fixed point DSP based on ADSP 2171 core.
- Fast arithmetic unit (38.5ns cycle).
- High-performance peripherals (double-update PWM modulators, flash A/D 12 bit converters, etc..).
- Suited for single-chip high-performance motion control applications.

Control Program Flow-Chart



- Implementation on ADMC401
- The control program is written in assembly language.
- The use of DFT based filters greatly simplifies the implementation.
- Execution times are short.

DSP Implementation

Program sample

```
.MODULE/RAM/SEG=USER_PM1      DFT_FILTER200;
.CONST    ORD_N=200;
.VAR/RAM/PM/CIRC  Filt_Coef[ORD_N];

#include "dft.dat"                        /* coefficients
                                             initialization   */
.ENTRY    DFT200;

DFT200:
        i5=^Filt_Coef;          /* use dedicated  */
        l5=%Filt_Coef;          /* circular registers */
        m5=1;                   /* i,l,m (0-7) */
        l0=%Filt_Coef;          /* i0 data pointer (same lenght) */
```

DSP Implementation

Program sample

```
m1=1;
mr = 0, mx0 = dm(i0,m1), my0 = pm(i5,m5);

cntr=%Filt_coef-1;

do calc0 until ce;
calc0: mr = mr + mx0 * my0 (ss),
            mx0 = dm(i0,m1), my0 = pm(i5,m5);
mr = mr + mx0 * my0 (rnd);

if mv sat mr;
rts;

.ENDMOD;
```

DSP Implementation
Program sample

- The algorithm exploits the same data structures (circular registers) used for DFT computation.
- The managing of these structures is different with respect to the DFT case.
- The DSP is optmized to implement such an algorithm in minimum time.
- Great accuracy and good performance can be achieved with reduced computation time.

Experimental Setup

Prototype ratings:

• DC-link voltage	300V
• Filter Inductance	1 mH
• Output Filter Capacitor	120µF
• Switching frequency	10kHz
• Selected frequencies:	3rd, 5th,7th,9th,11th

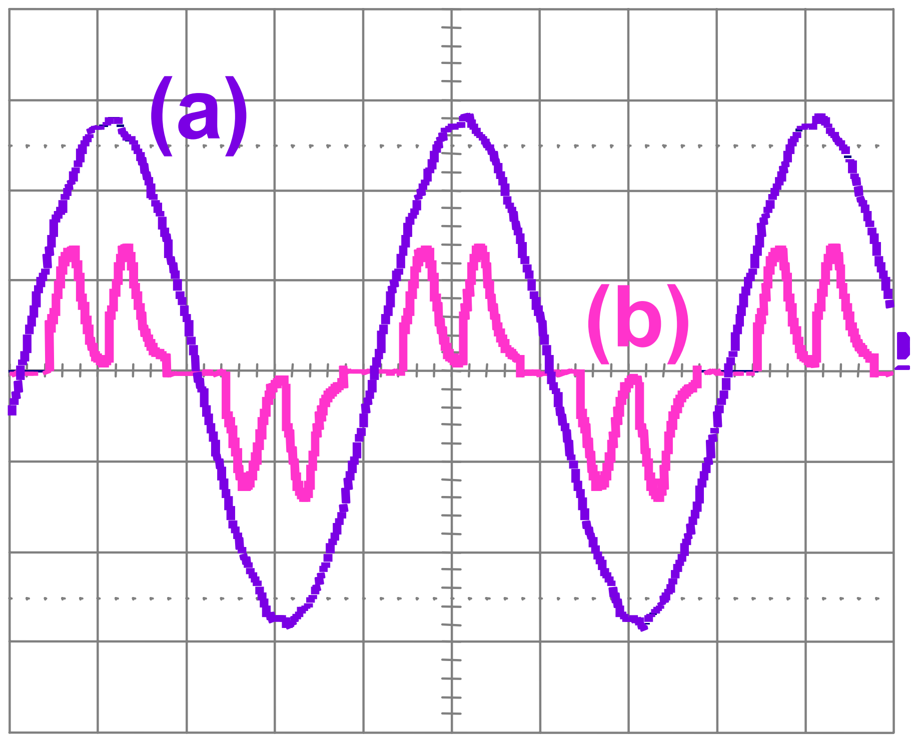
Experimental Results

Three-phase diode rectifiers - Proposed solution

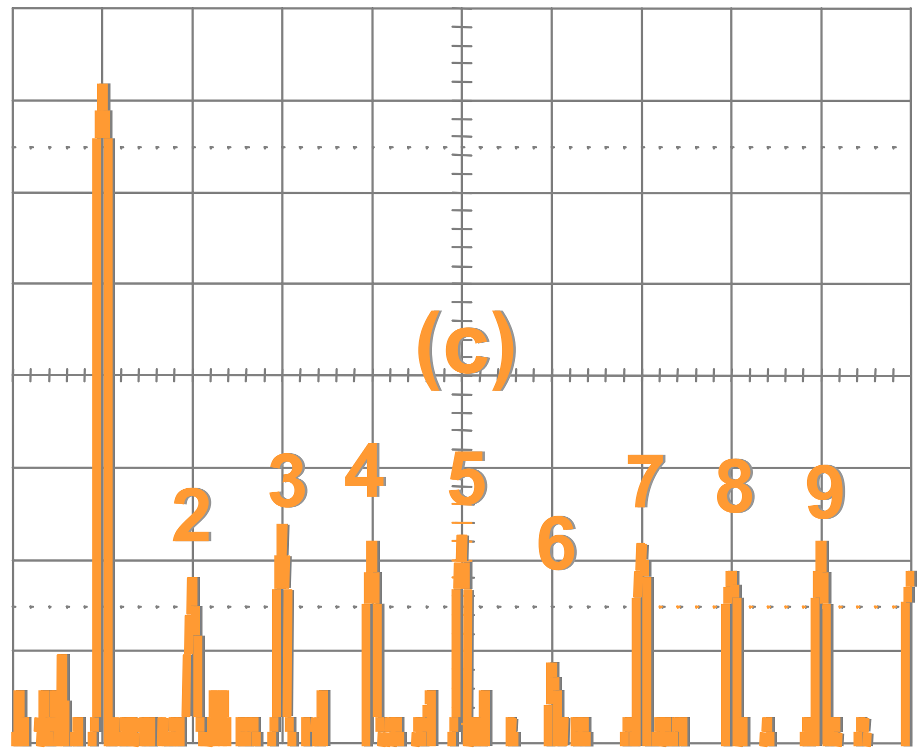
(a) Ouput Voltage (40V/div)

(b) Ouput current (10A/div)

c) Output voltage spectrum (10dB/div)



time (5ms/div)



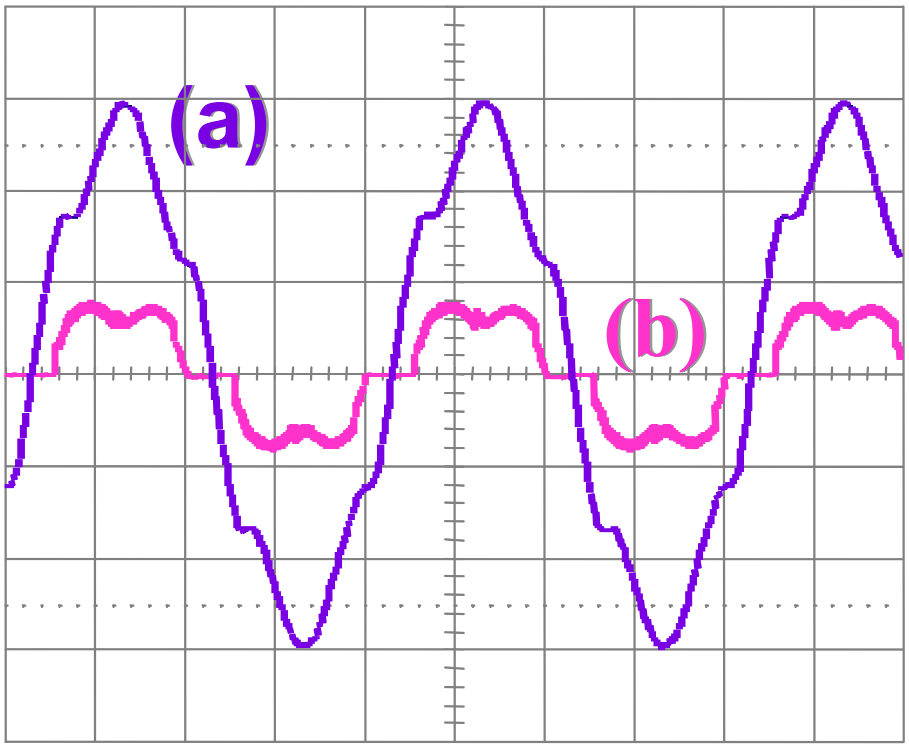
frequency (50Hz/div)

Experimental Results

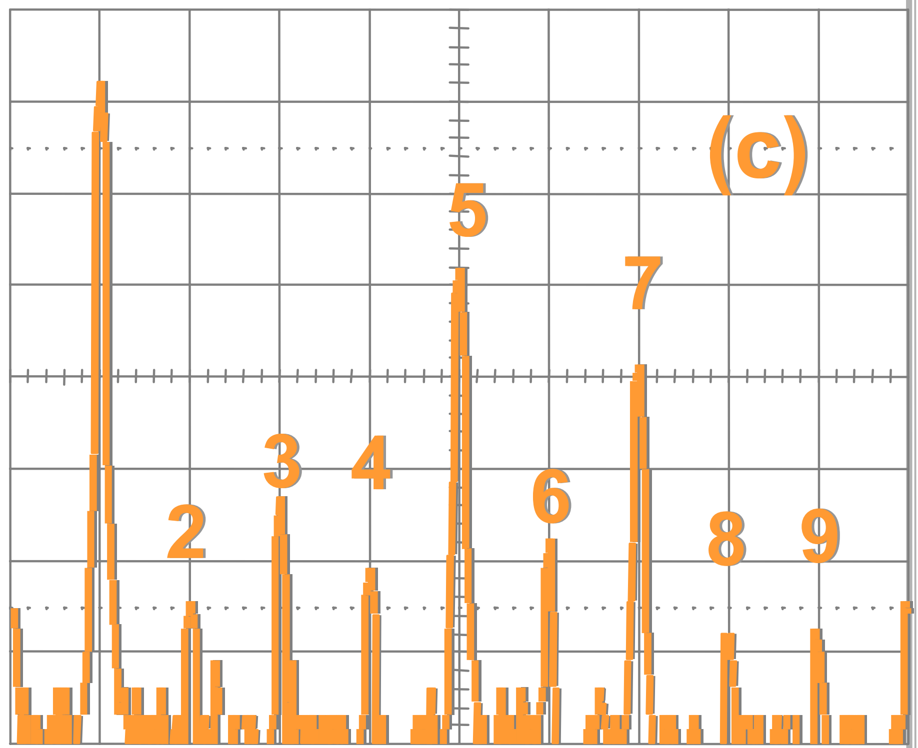
Three-phase diode rectifiers - PI controller

(a) Ouput Voltage (40V/div)
(b) Ouput current (10A/div)

c) Output voltage spectrum (10dB/div)



time (5ms/div)

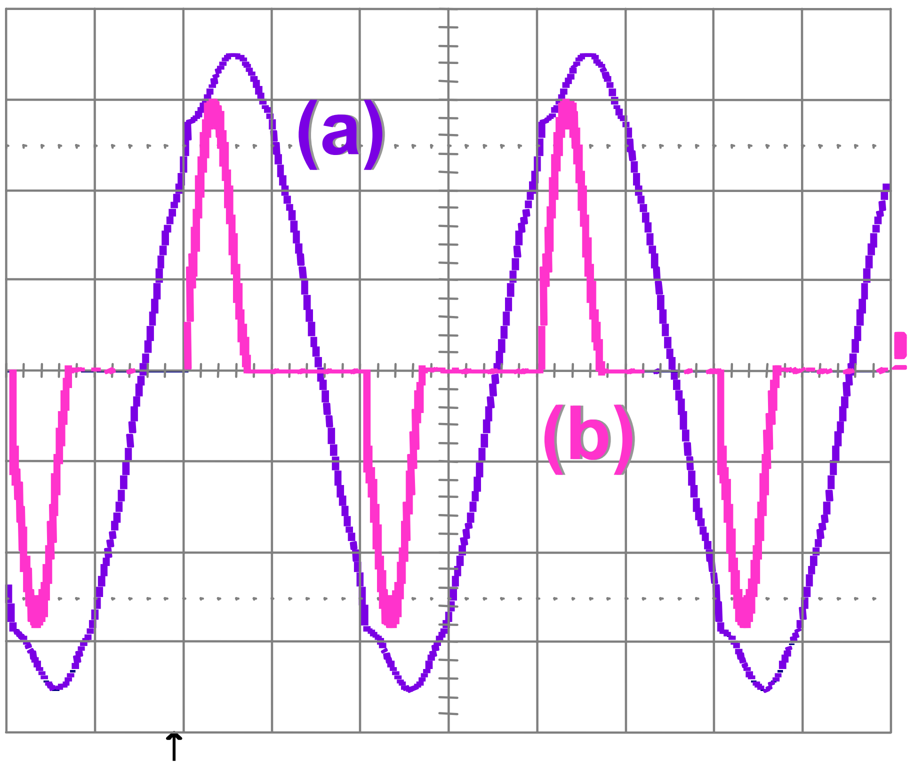


frequency (50Hz/div)

Experimental Results
Single-phase diode rectifier

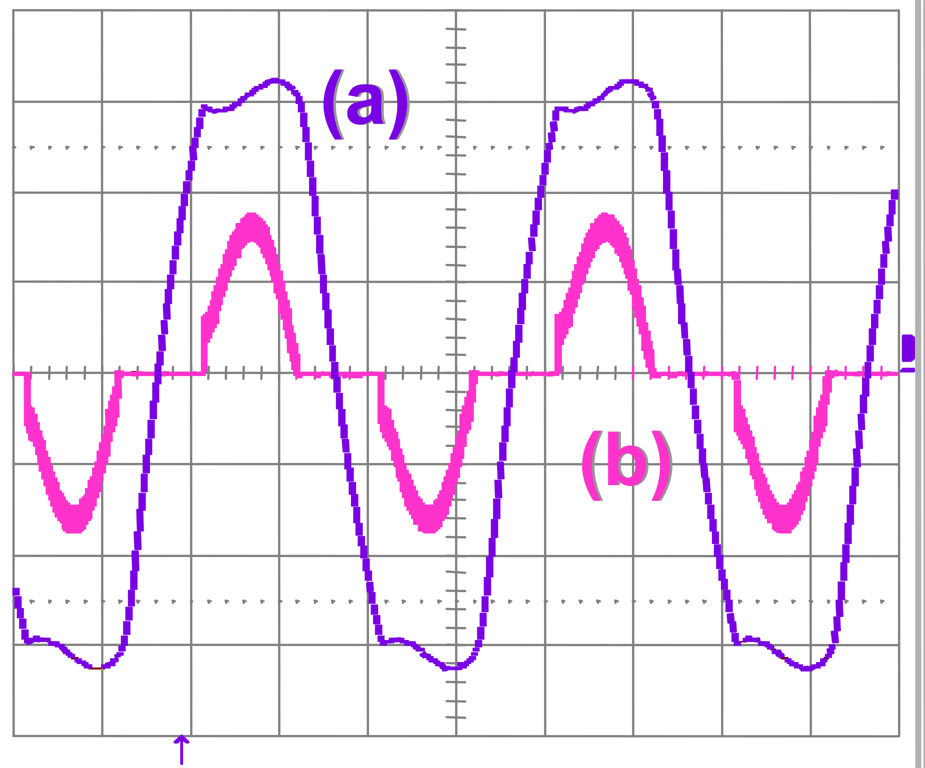
(a) Ouput Voltage (40V/div) **(b) Ouput current (5A/div)**

Proposed solution



time (5ms/div)

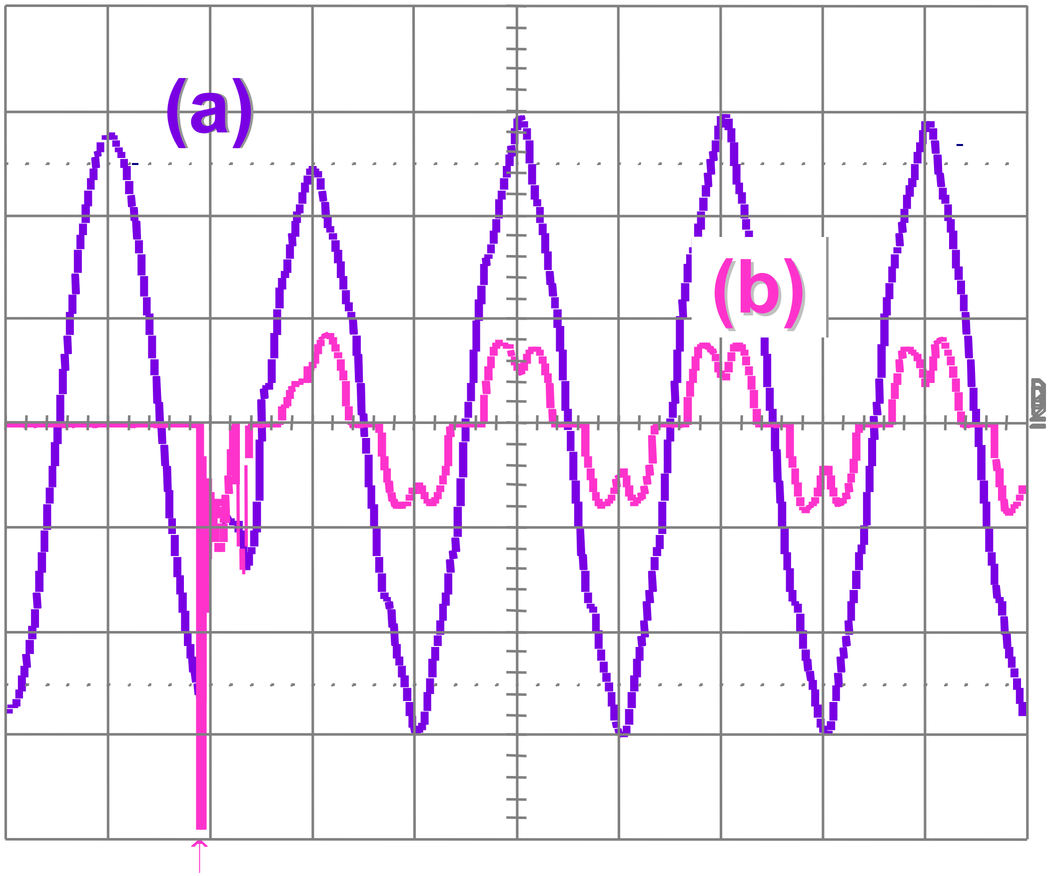
Conventional PI



time (5ms/div)

Experimental Results
Distorting Load Turn-on

(a) Ouput Voltage (40V/div) (b) Ouput current (10A/div)



time (10ms/div)

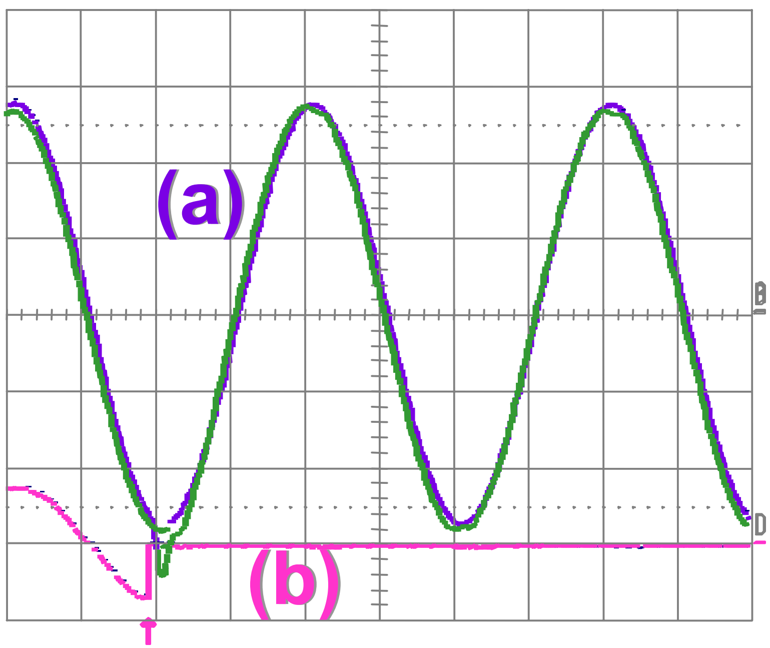
Experimental Results

Linear Load Step-Changes

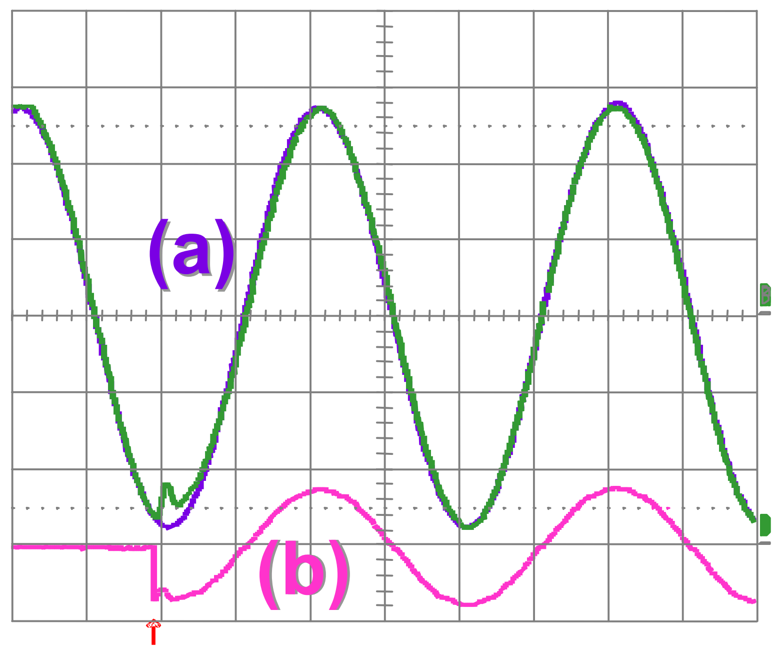
Turn-off **Turn-on**

(a) Ouput Voltage and its reference (40V/div)

(b) Ouput current (5A/div)



time (5ms/div)



time (5ms/div)

Reference

P. Mattavelli, S. Fasolo: "Implementation of Synchronous Frame Harmonic Control for High-Performance AC Power Supplies", IEEE IAS Annual Meeting 2000, Rome, Italy, 8-12 October, 2000, pp. 1988-1995.