Lesson 3

Digitally-Controlled Single-Phase AC/DC Integrated PWM Converter

Goal of the work

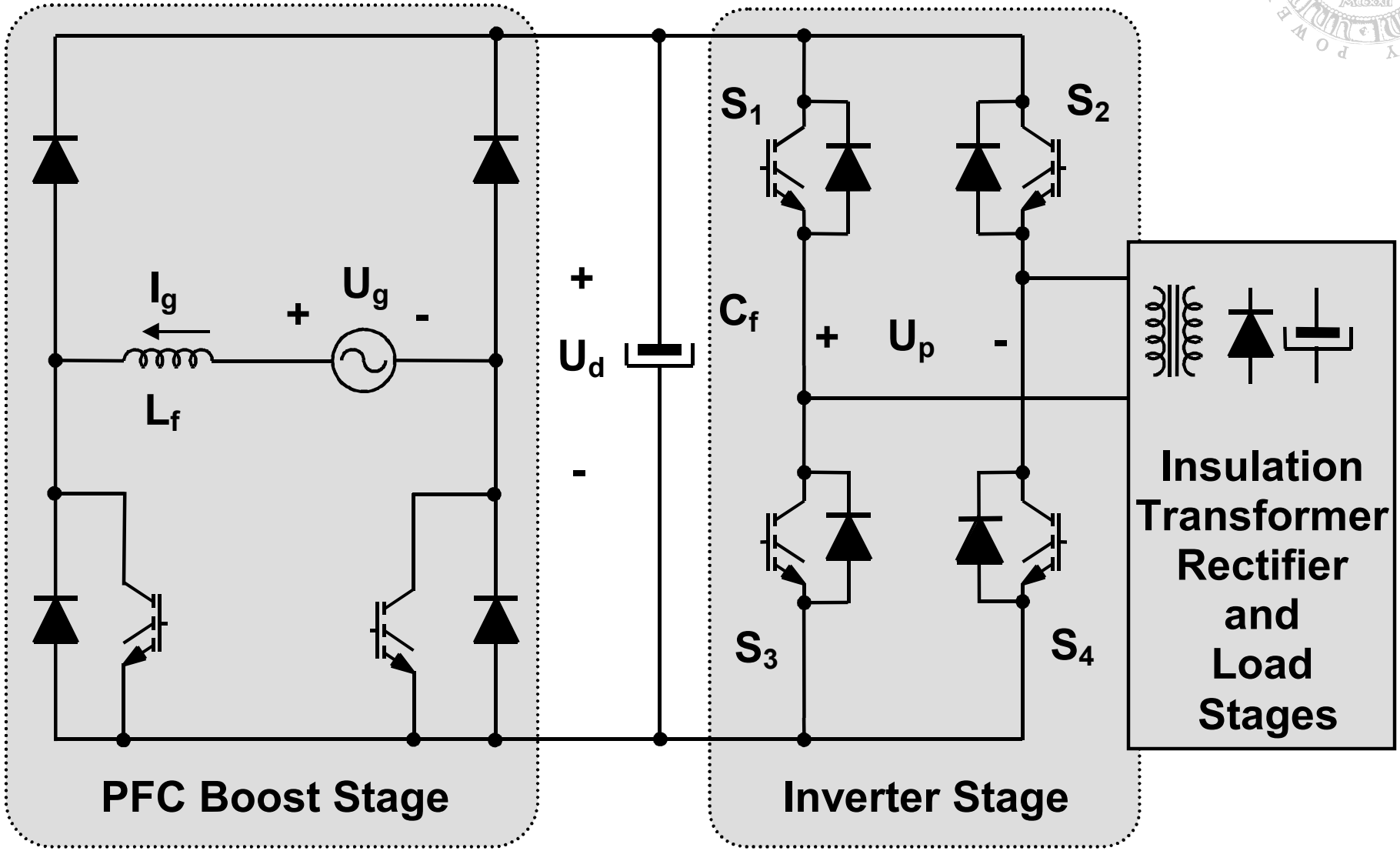
Development of a new topology of single phase insulated ac/dc converter featuring:

- **high power factor**
- **full control of the output dc voltage**
- **high-frequency insulation transformer**
- **high-frequency line filter inductor.**

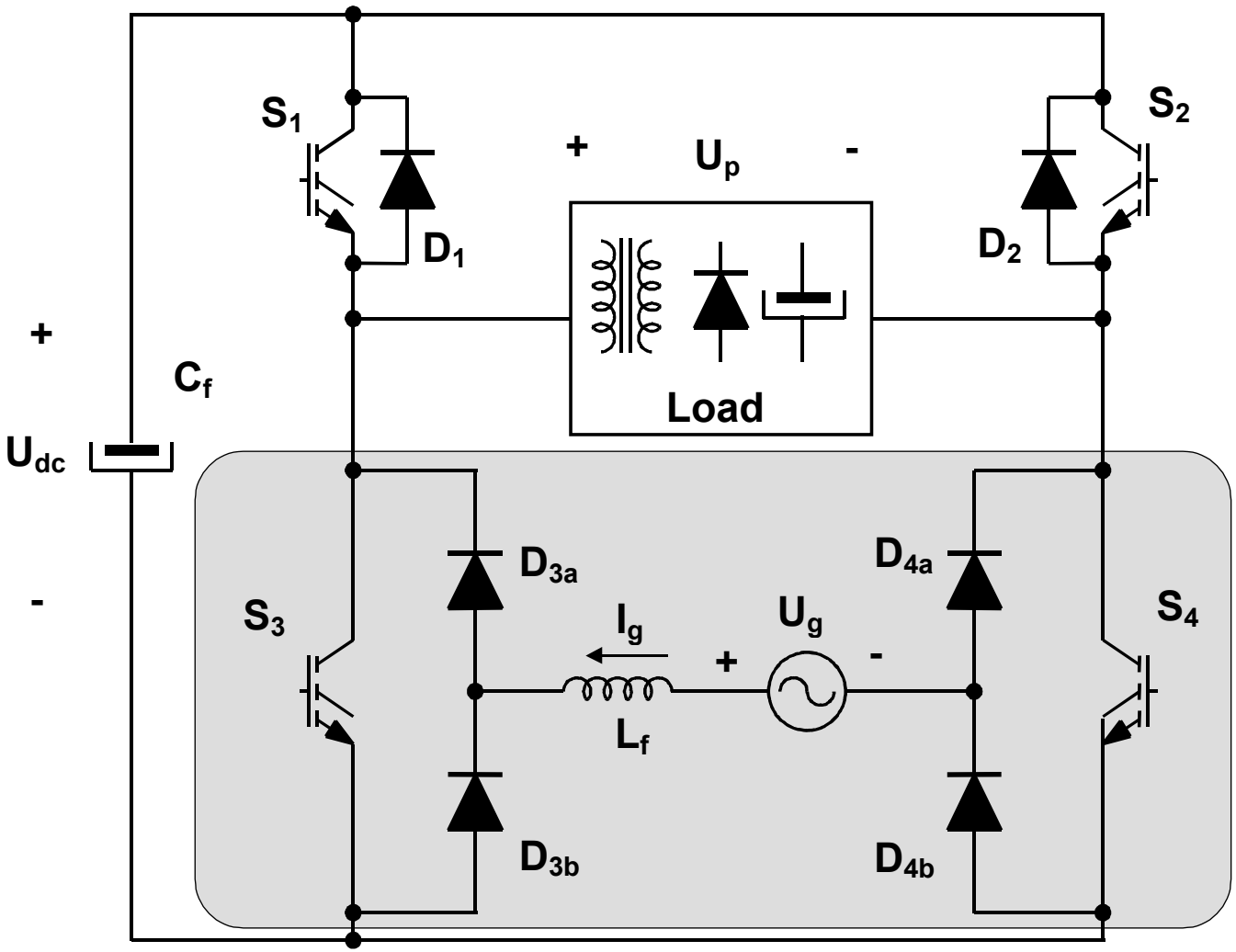
Presentation Outline

- Converter topology
  - operation modes
  - structural constraints
- Design procedure
- Control strategy
  - analog control
  - digital control
- Experimental results

Basic AC/DC Topology



Integrated Converter Topology

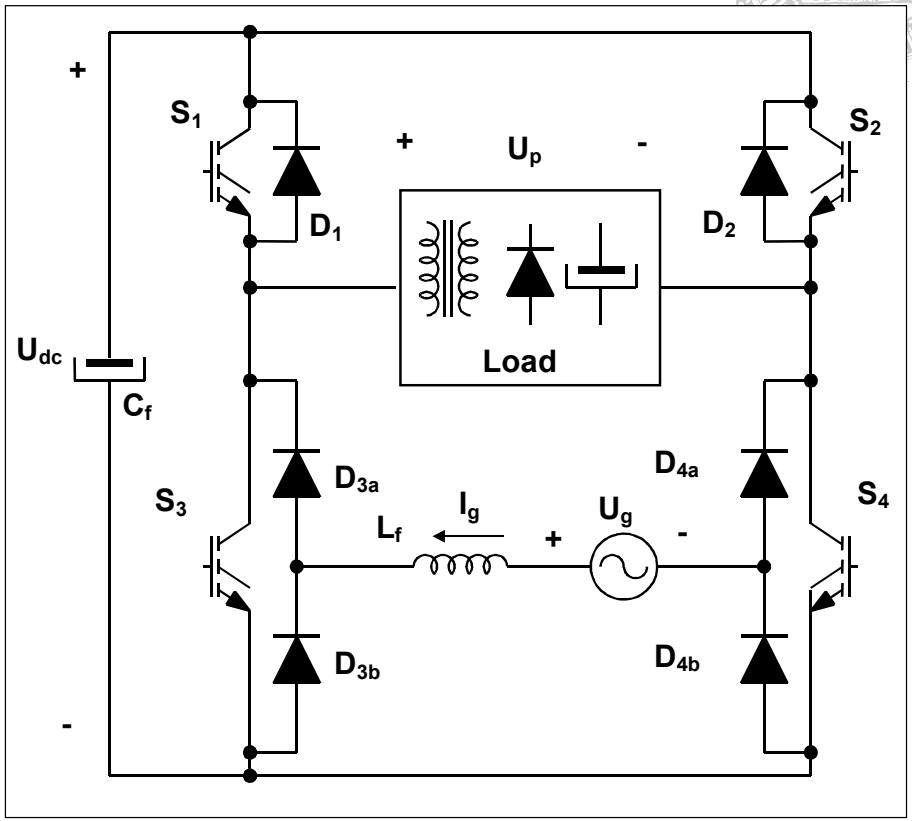


Converter Modes of Operation

Switches are driven so as to generate powering and free-wheeling phases.

Free-wheeling phases are obtained closing the two high-side or the two low-side switches.

The two free-wheeling phases have opposite effect on the converter input current thus allowing control of the current waveform.



The converter integrates the PFC and inverter stages but loses some degree of control. This limits the line (or load) side performance.

Converter Operation Table

Switches ON	Diodes ON	U_g	U_p	I_g
S_1-S_2	D_1, D_{3a}, D_{4b}	> 0	0	decrease
S_3-S_4	D_{3a}, D_{4b}	> 0	0	increase
S_1-S_4	(D_1), D_{3a}, D_{4b}	> 0	$+U_{dc}$	decrease
S_2-S_3	D_{3a}, D_{4b}	> 0	$-U_{dc}$	increase
S_1-S_2	D_2, D_{3b}, D_{4a}	< 0	0	increase
S_3-S_4	D_{3b}, D_{4a}	< 0	0	decrease
S_1-S_4	D_{3b}, D_{4a}	< 0	$+U_{dc}$	decrease
S_2-S_3	(D_2), D_{3b}, D_{4a}	< 0	$-U_{dc}$	increase

Operation Constraints

- The duration of the powering phases must be the same to avoid output transformer saturation.
- The modulation period, T_{sw}, is then divided into three phases:
  - positive powering phase: duration $M/2 \cdot T_{sw}$
  - negative powering phase: duration $M/2 \cdot T_{sw}$
  - free-wheeling phase: duration $(1 - M) \cdot T_{sw}$
- During the free-wheeling phase, input current control is possible.

Operation Constraints

The input current can be controlled only during the free-wheeling phases of the load side control.

When the modulation index M is high, the available time for the input current control is small.

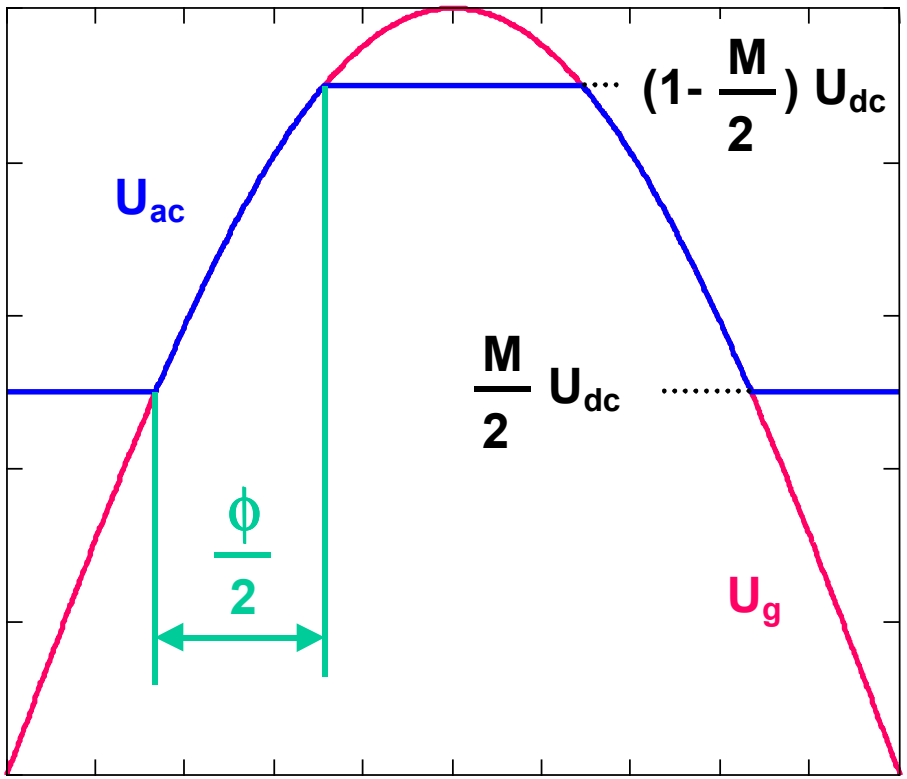
$$M = \frac{U_o}{U_{dc}}$$

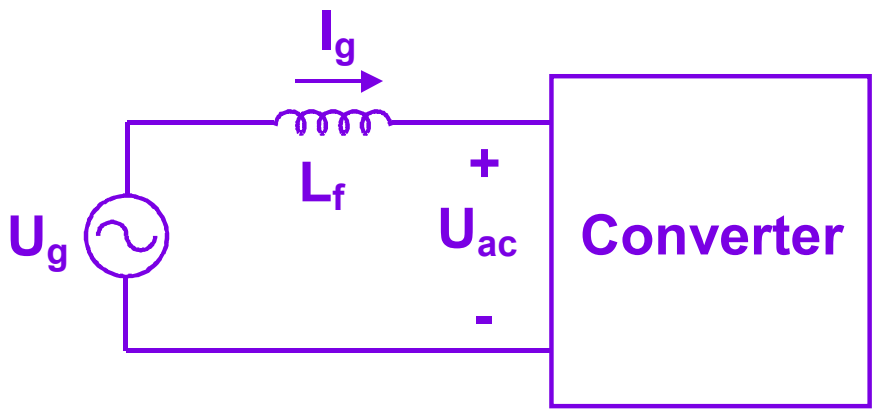
The input current control is possible only when:

$U_{gmin} < |U_g(\theta)| < U_{gmax}$, where

$$\begin{cases} U_{gmin} = \dfrac{M}{2} \cdot U_{dc} \\ U_{gmax} = \left(1 - \dfrac{M}{2}\right) \cdot U_{dc} \end{cases}$$

Operation Constraints

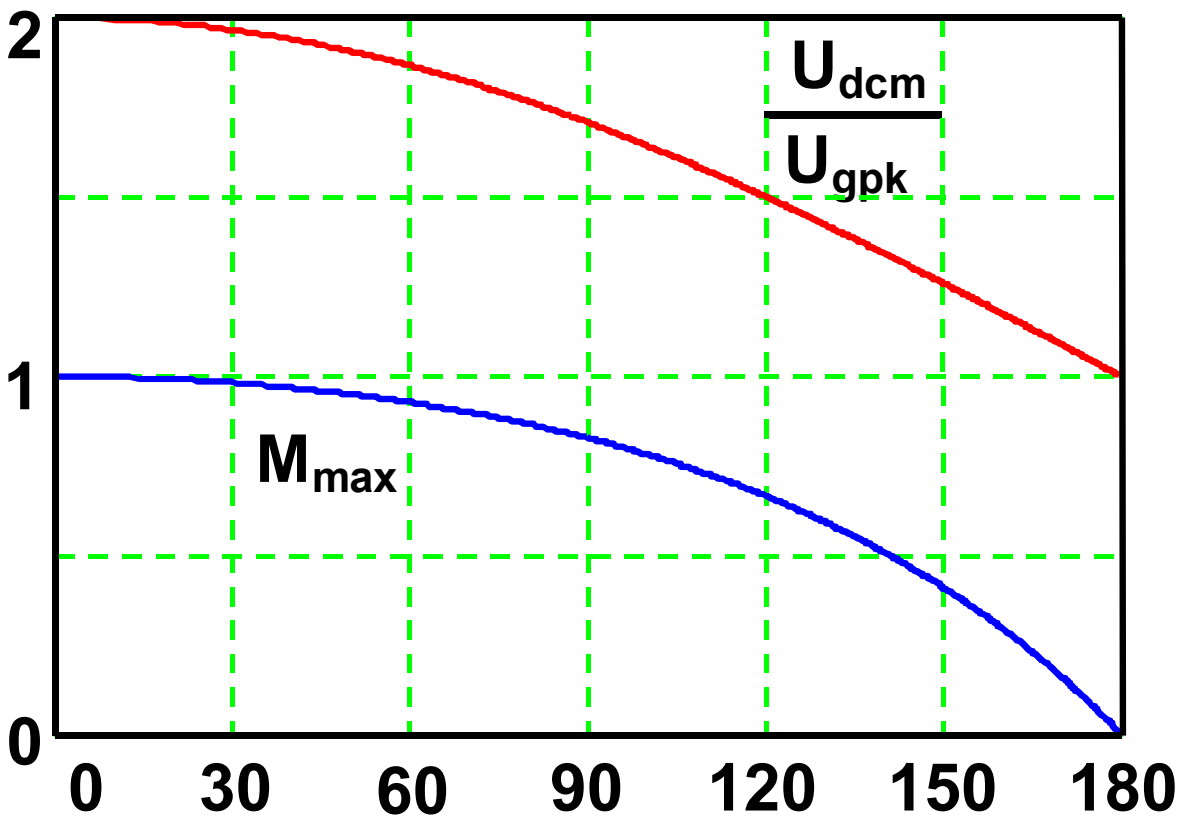




Average ac voltage at converter input and corresponding input current control angle ϕ

Operation Constraints

Maximum allowed duty-cycle M and dc link voltage to peak input voltage ratio as a function of the line current control angle ϕ



$\phi = 120°$

$M_{MAX} = 0.67$

$U_{dc\_max} = 1.5\ U_{g\_pk}$

Converter Design

From the previous graphs the following design procedure can be adopted:

- Select maximum dc link voltage, based on switches' voltage rating;
- Given the peak line voltage, the design diagram allows to determine the maximum achievable M value;
- The same diagram also allows to determine the line control angle ϕ, that should be equal or higher than 120°, to get a satisfactory PF and current THD.

Converter Design

Passive components' selection:

- Given the desired input current ripple, input inductance is given by:

$$L_f = \frac{U_{dc}}{4 \cdot f_{sw} \cdot \Delta I_{Lpp}}$$

U_{dc} = dc link voltage

- Given the desired low frequency output voltage ripple, the dc link capacitor can be selected according to:

$$C_f = \frac{P_{out}}{2 \cdot \pi \cdot f_{line} \cdot \Delta U_{dcpp} \cdot U_{dc}}$$

P_{out} = output power

Converter Design

The maximum stresses for the active components are:

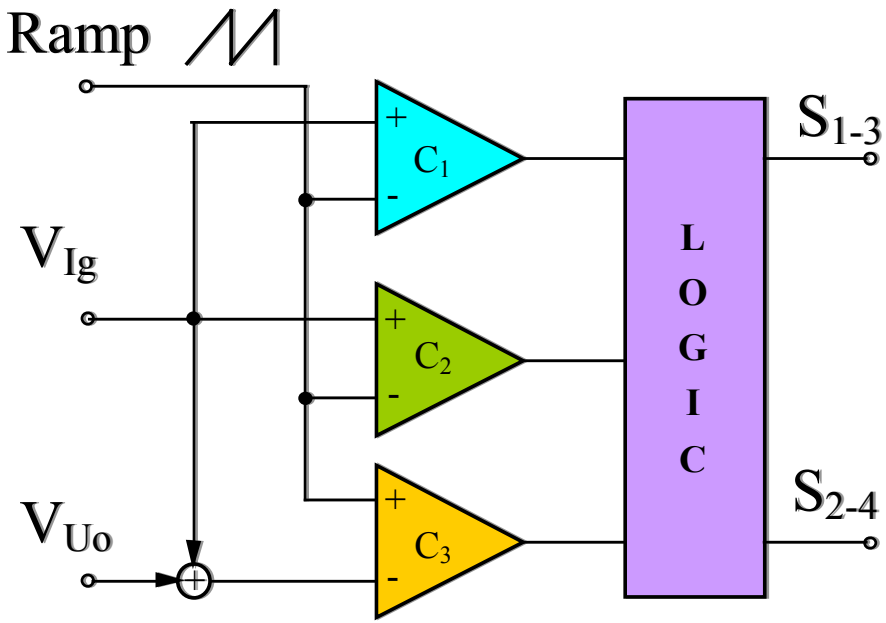
- Voltage stress equal to the DC link voltage
- Current stress for the upper switches as in any standard inverter
- Current stress for the lower switches and diodes is the sum of inverter load side and line side currents

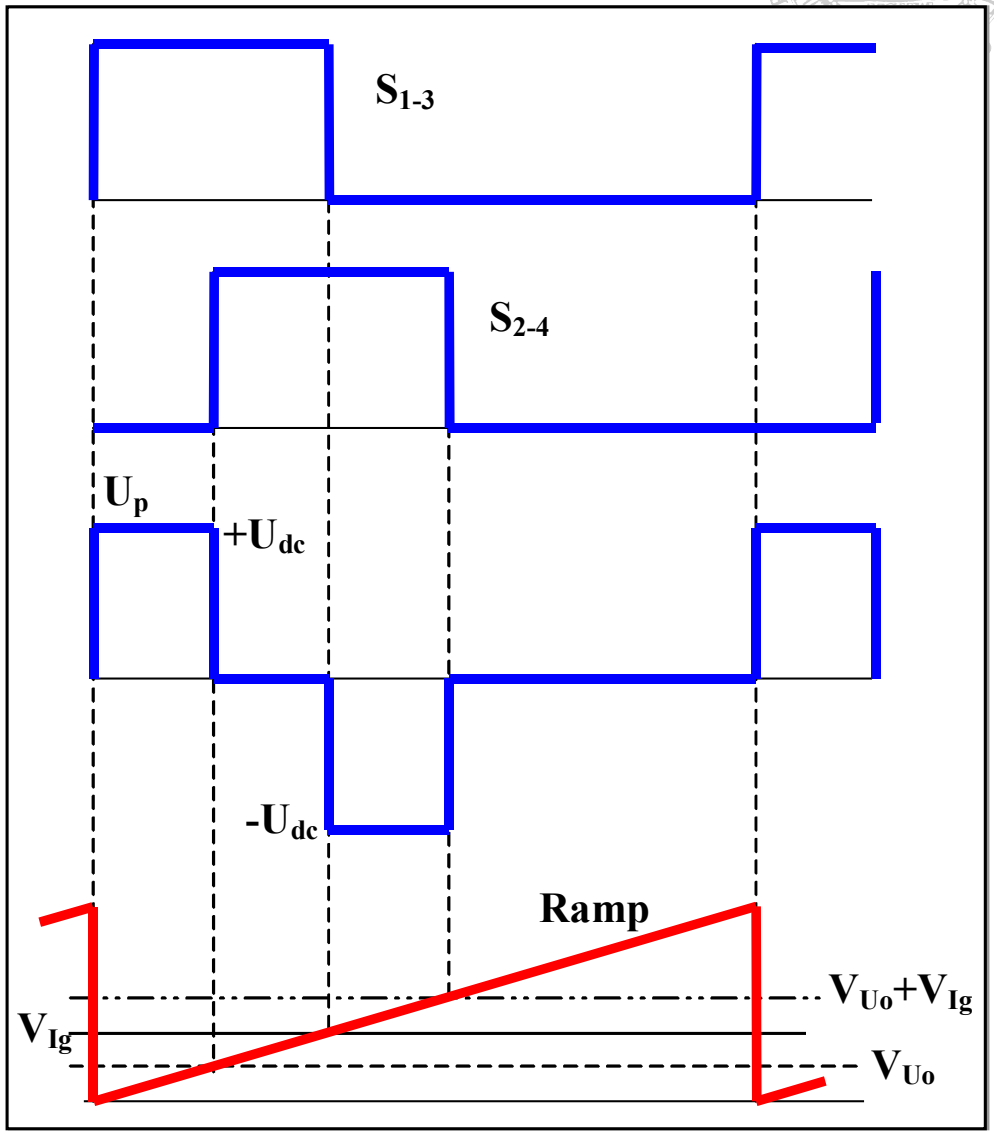
Converter Control

- We considered both an analog and a digital control technique.
- The analog solution is based on a standard PFC controller and on a modified phase-shift modulator for full-bridge converters.
- The digital solution is based on a dead-beat type of control equation and on a custom digital PWM modulator.
- In both cases the output voltage may be controlled by a standard regulator (e.g. PID).

Analog Converter Control

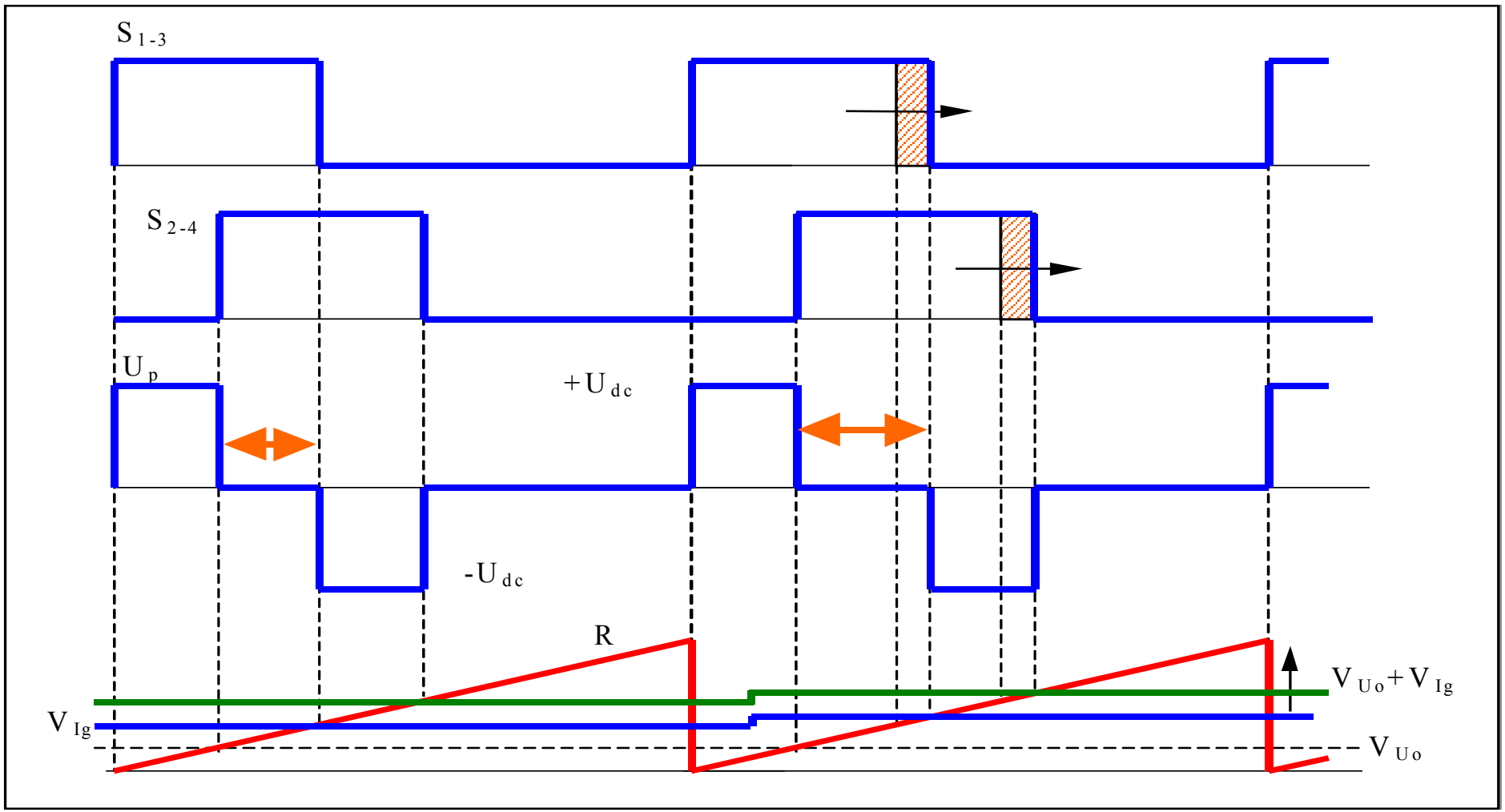
Analog PWM modulator



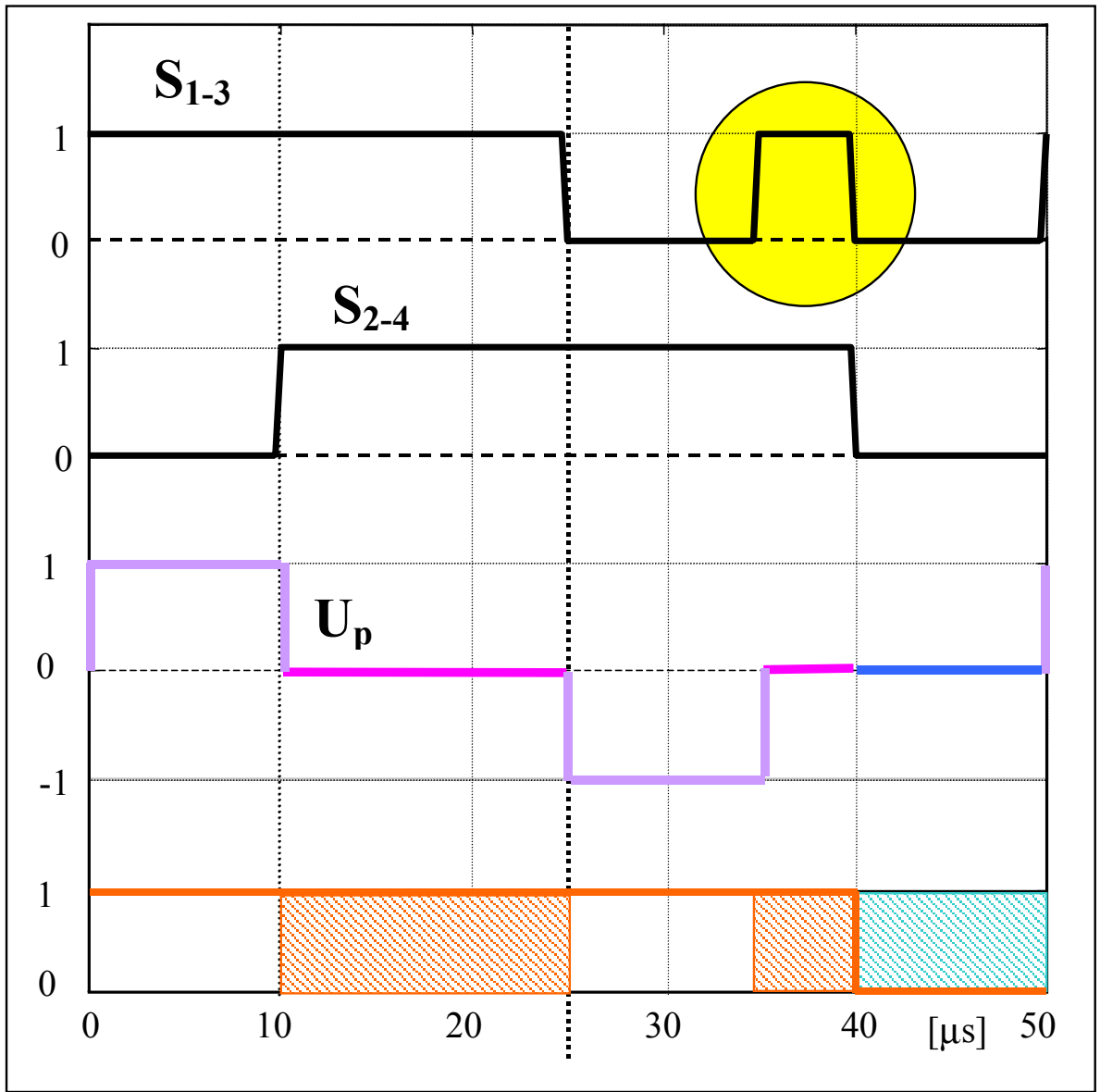


Analog Converter Control

Control of the free-wheeling phase



Analog Converter Control



Symmetrical positioning of switching pulses requires two additional commutations

Analog Converter Control

- The input variables of the PWM modulator, i.e. V_{Uo} and V_{Ig}, must be provided by the output voltage and input current regulators.
- The output voltage regulator may be any of those used for forward converters. A simple solution might be voltage mode control with PID regulator.
- The input current regulator may be a standard average current PFC controller with analog multiplier.

Digital Converter Control

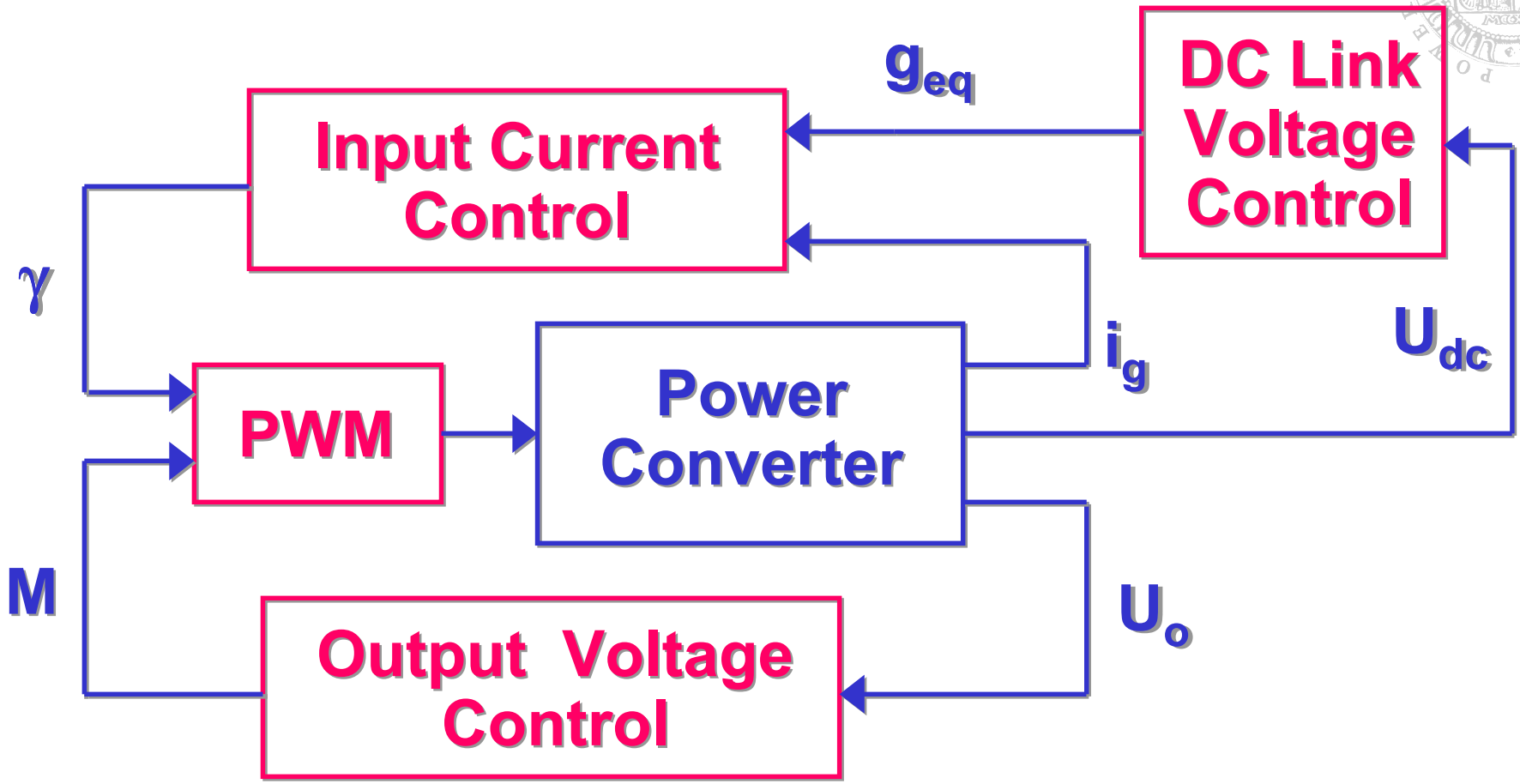
- Digital implementation requires significant computational power to allow input current, DC link voltage and output voltage control.
- Flexibility in the PWM modulator is required to implement the non-standard modulation strategy.
- Texas Instruments TMS320F240 DSP is the hardware platform selected for the practical implementation.

Digital Converter Control

The control system is organized as follows:

- Digital PWM
- Input current control loop
- Output voltage control loop (not implemented)
- DC link voltage control loop

Digital Converter Control

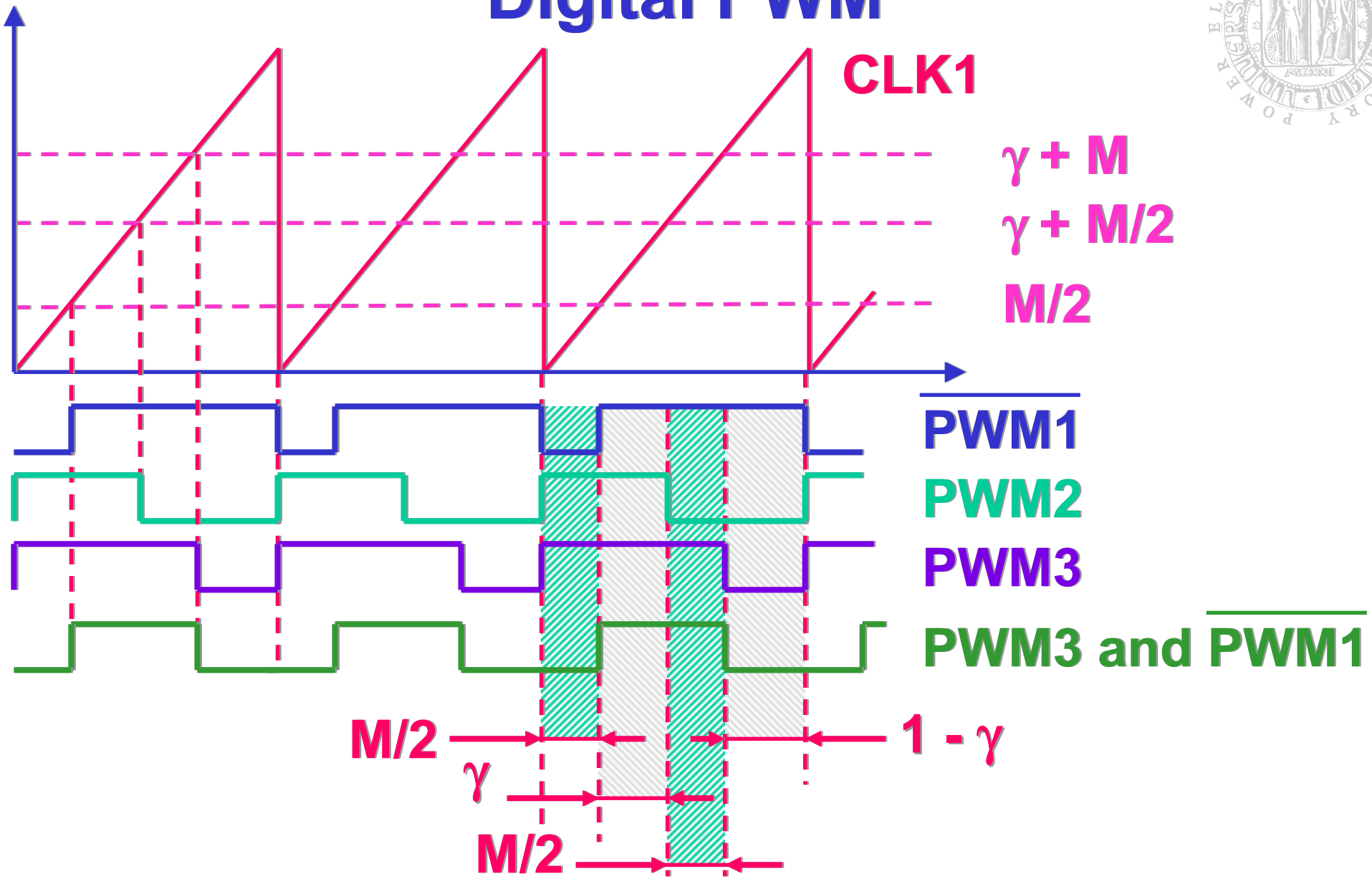


Digital control block diagram

Digital PWM

- The PWM implementation uses one of the three DSP internal counters. It is programmed for a period of 50 μs (20kHz).
- Three PWM outputs are used to generate the logic state of two inverter legs.
- The CMP input registers of the PWM units are loaded with values which are related to the load duty-cycle (M) and line "duty-cycle" γ.
- The duty-cycles are generated by external loops (output voltage and line current loops).

Digital PWM



Digital PWM

- This solution allows simultaneous and independent variation of the input variables.
- Its response time is equal to one modulation period (worst case).
- The constraint

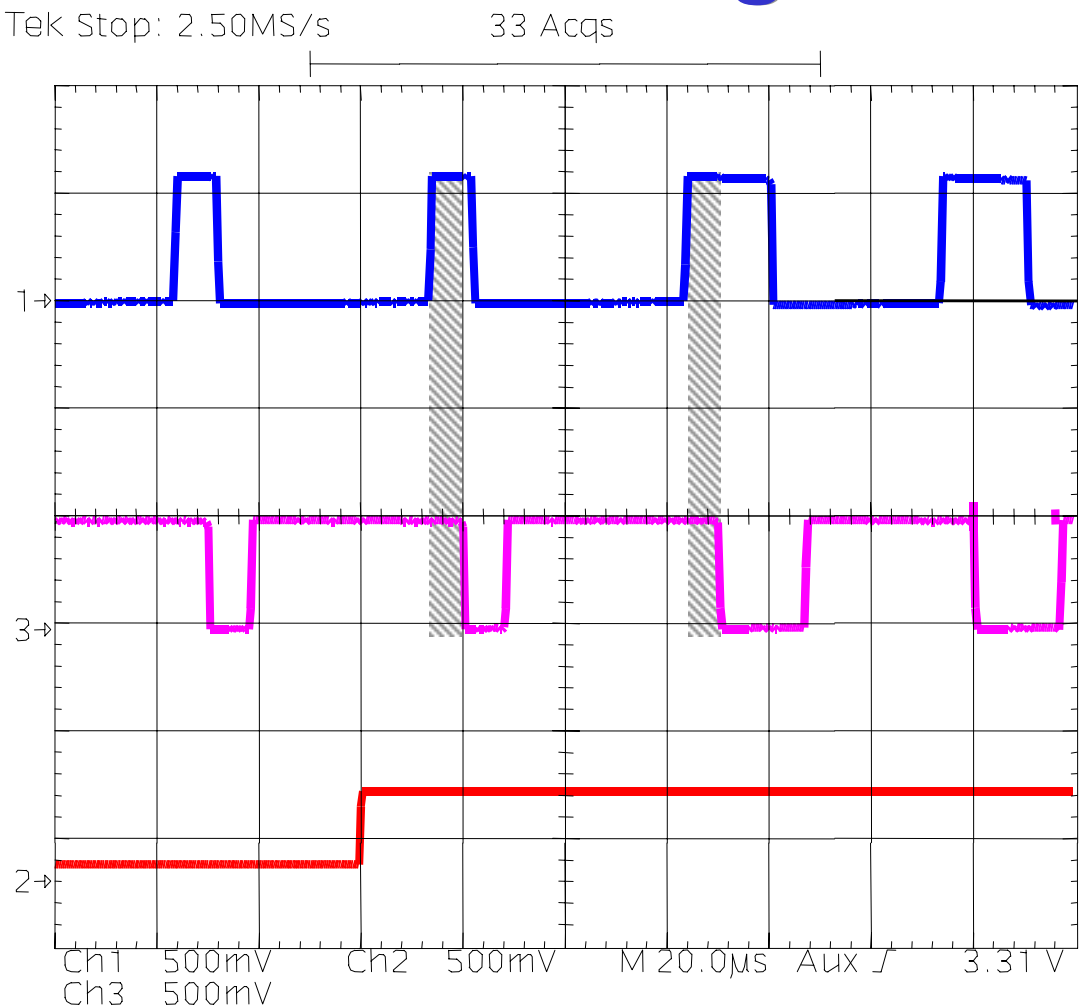
$$\gamma_{max} = 1 - M$$

requires the definition of a strategy to deal with the interactions between the two loops.

Digital PWM

- The strategy we applied is to give the highest priority to the output voltage control loop.
- When the output voltage controller requires a sudden variation of the parameter M, this is performed even if input current control is lost.
- The input current controller must be capable of tolerating this momentary control losses without generating persisting oscillations and/or instabilities.
- These problems arise only in the presence of transients at the load side.

Digital PWM



$S_{1\text{-}3}$ logic state

$S_{2\text{-}4}$ logic state

M step variation

Dynamic response of the PWM modulator

Input current control

- The input current dynamic equation is the following:

$$i_g(t) = \frac{1}{L_f} \cdot \int_0^t U_{Lf}(\tau)d\tau = \frac{1}{L_f} \cdot \int_0^t U_g(\tau) - U_{ac}(\tau)d\tau$$

- This can be discretized by assuming the voltage to be constant between sampling instants (zero order hold discretization).

Input current control

- The input inductor average voltage in a modulation period can be easily found to be:

$$U_{Lf} = U_g - U_{dc} \cdot [M/2 + \delta \cdot (1 - M)]$$

- Consequently, the current variation in a modulation period is given by:

$$i_g(k+1) - i_g(k) = U_g(k) \cdot \frac{T_{sw}}{L_f} + -\left[\frac{M}{2} + \delta(k) \cdot (1 - M)\right] \cdot U_{dc}(k) \cdot \frac{T_{sw}}{L_f}$$

Input current control

- The quantity $\delta \cdot T_{sw}$ is the duration of the upper (or positive) free-wheeling phase.
- It is possible to calculate $\delta(k+1)$ so as to force the current i_g to reach its reference at instant k+2.
- This generates the following control equation:

$$\delta(k+1) = -\delta(k) - \left[g_{eq} \cdot \left|U_g(k)\right| - \left|i_g(k)\right|\right] \cdot \frac{L_f}{T_{sw} \cdot U_{dc} \cdot (1-M)} + \frac{2 \cdot \left|U_g(k)\right|}{(1-M) \cdot U_{dc}} - \frac{M}{1-M}.$$

Input current control

- The control equation assumes that

$$i_g(k+2) = g_{eq} \cdot U_g(k)$$

i.e. U_g is slowly varying with respect to the control period.

- G_{eq} is the converter equivalent input conductance. This is generated by the DC link voltage control loop.

Input current control

- The control equation is difficult to implement because it implies the execution of divisions.
- The variation of the DC link voltage can be neglected, i.e. $U_{dc} \cong$ constant.
- The variation of M can be dealt with defining a new control variable:

$$\gamma(k) = [1 - M(k)] \cdot \delta(k)$$

- While δ can vary from 0 to 1 γ can vary from 0 to 1-M.

Input current control

- The control equation can be re-written in terms of the γ variable.
- This way, only MAC instructions can be used.

$$\gamma(k+1) = -\gamma(k) - \left[g_{eq} \cdot \left|U_g(k)\right| - \left|i_g(k)\right|\right] \cdot \frac{L_f}{T_{sw} \cdot U_{dc}} + \frac{2 \cdot \left|U_g(k)\right|}{U_{dc}} - M(k).$$

- This is the implemented current control equation.
- The absolute value is required to deal with $U_g < 0$.

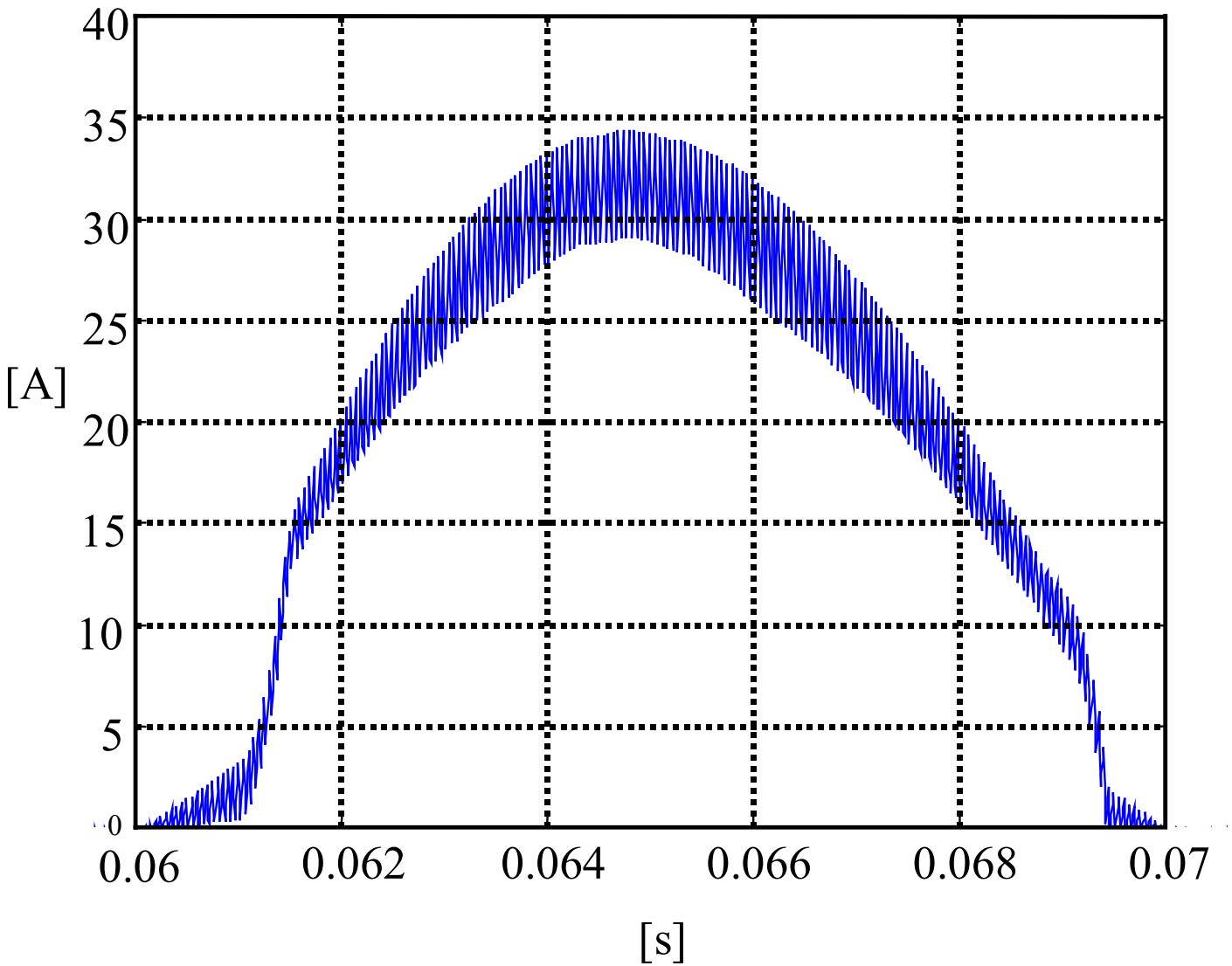
Current control simulation

Simulation of the proposed input current digital control was performed.

Converter Parameters

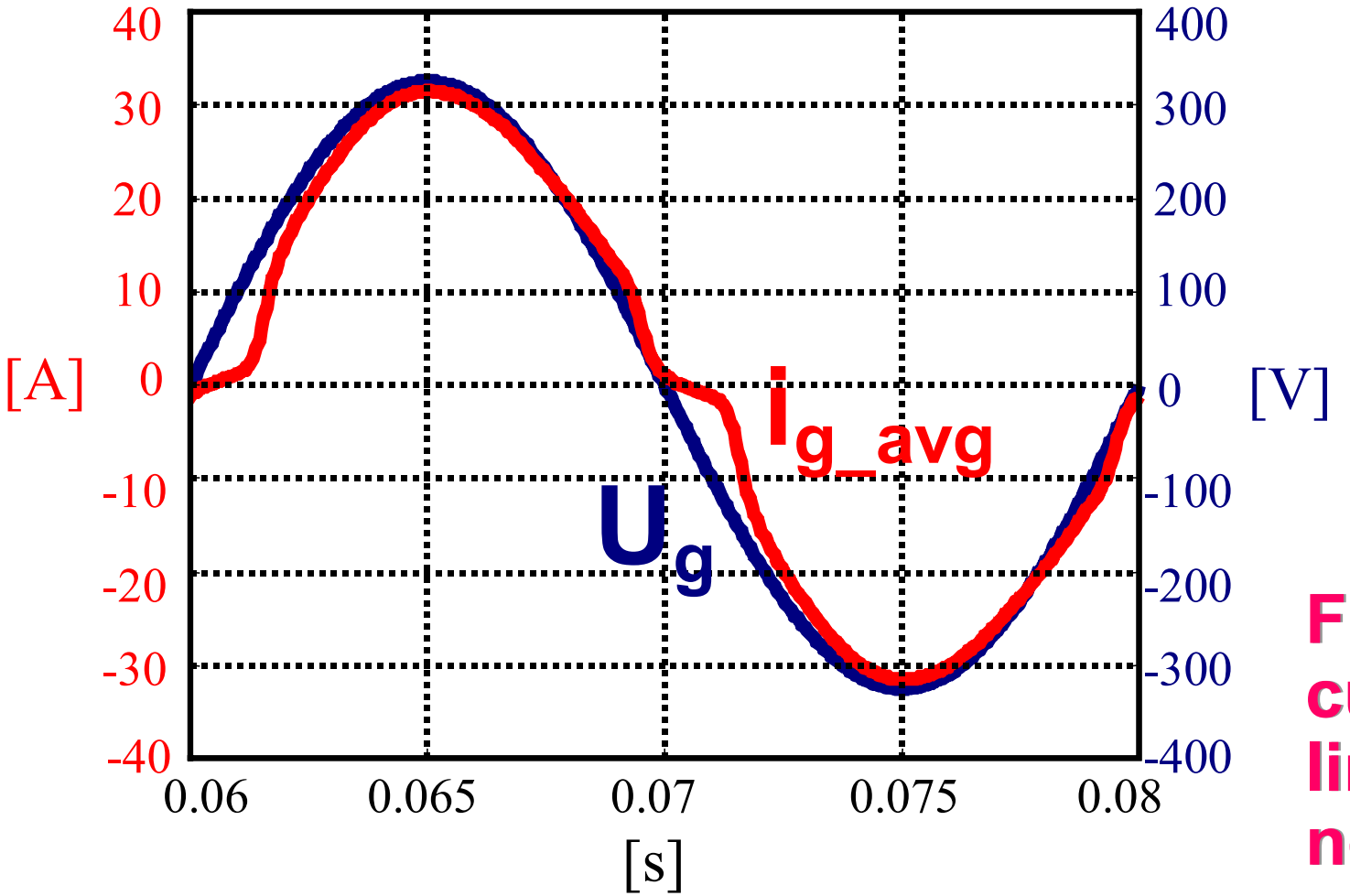
Line voltage	U_g	$240 \pm 10\%$	V_{RMS}
Output power	P_o	5	kW
Switching frequency	f_{sw}	20	kHz
Input inductor	L_f	1	mH
DC link capacitor	C_f	800	μF

Current control simulation



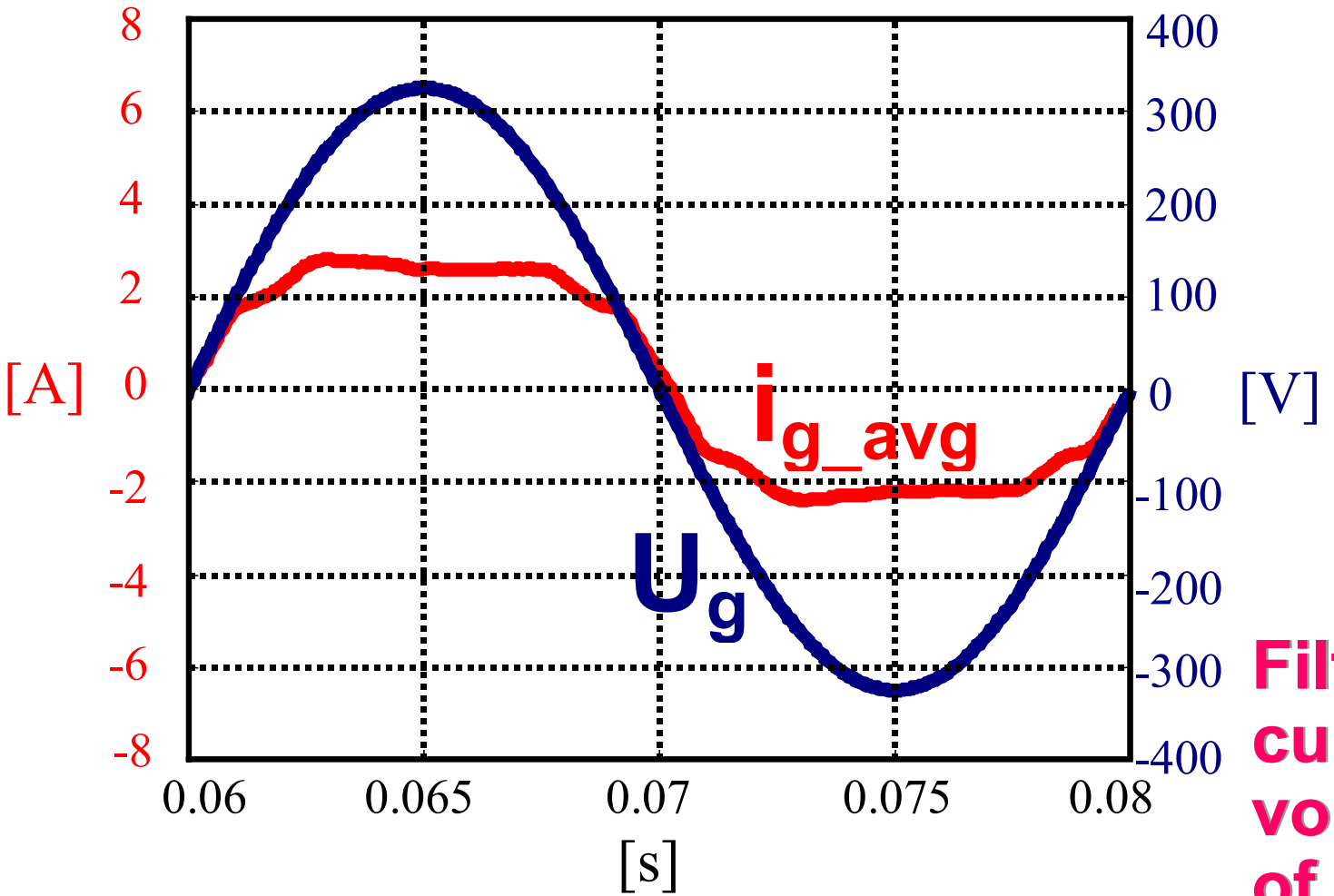
Input current in a line half-period

Current control simulation



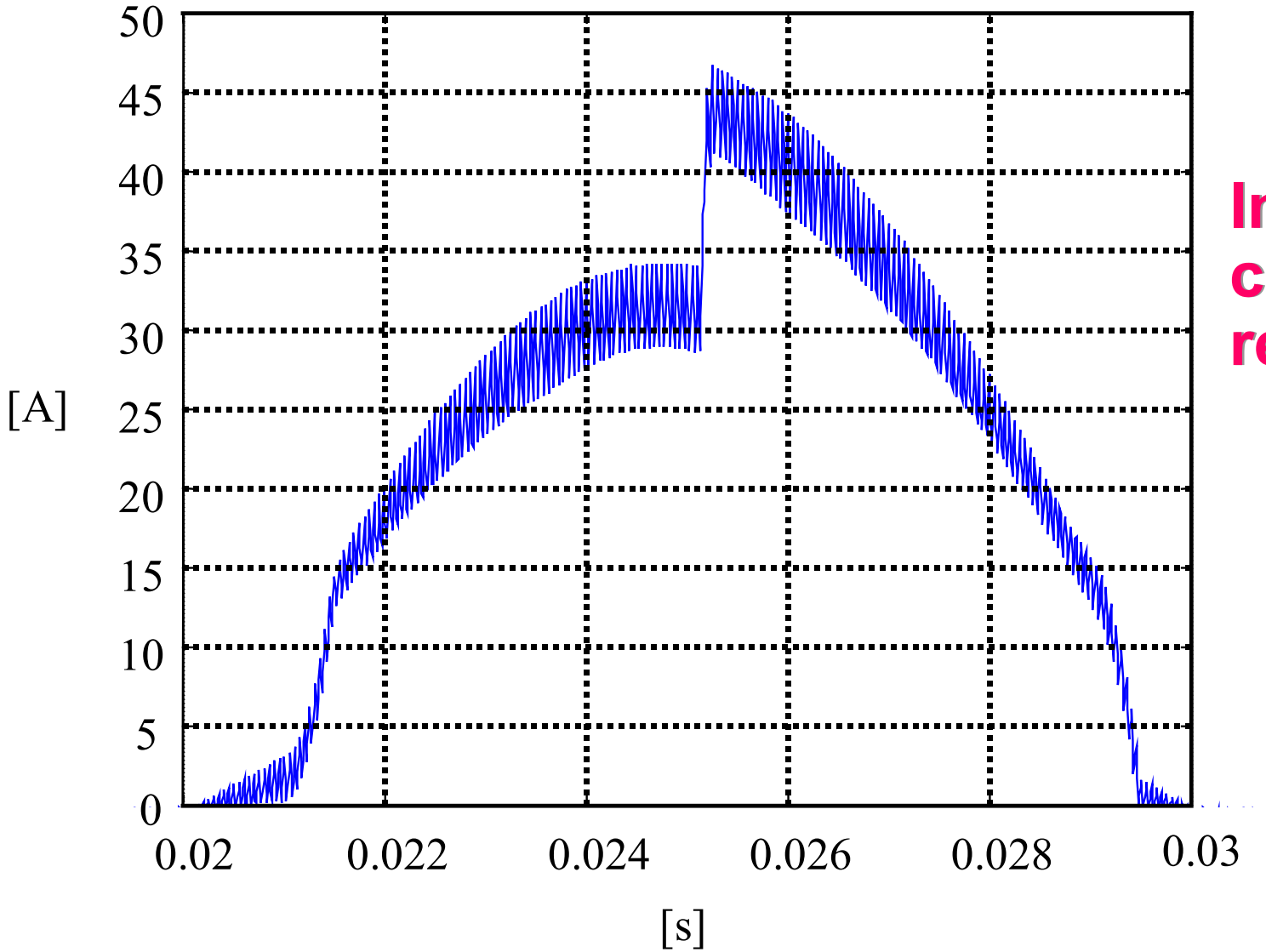
Filtered line current and line voltage at nominal output power

Current control simulation



Filtered line current and line voltage at 10% of nominal output power

Current control simulation

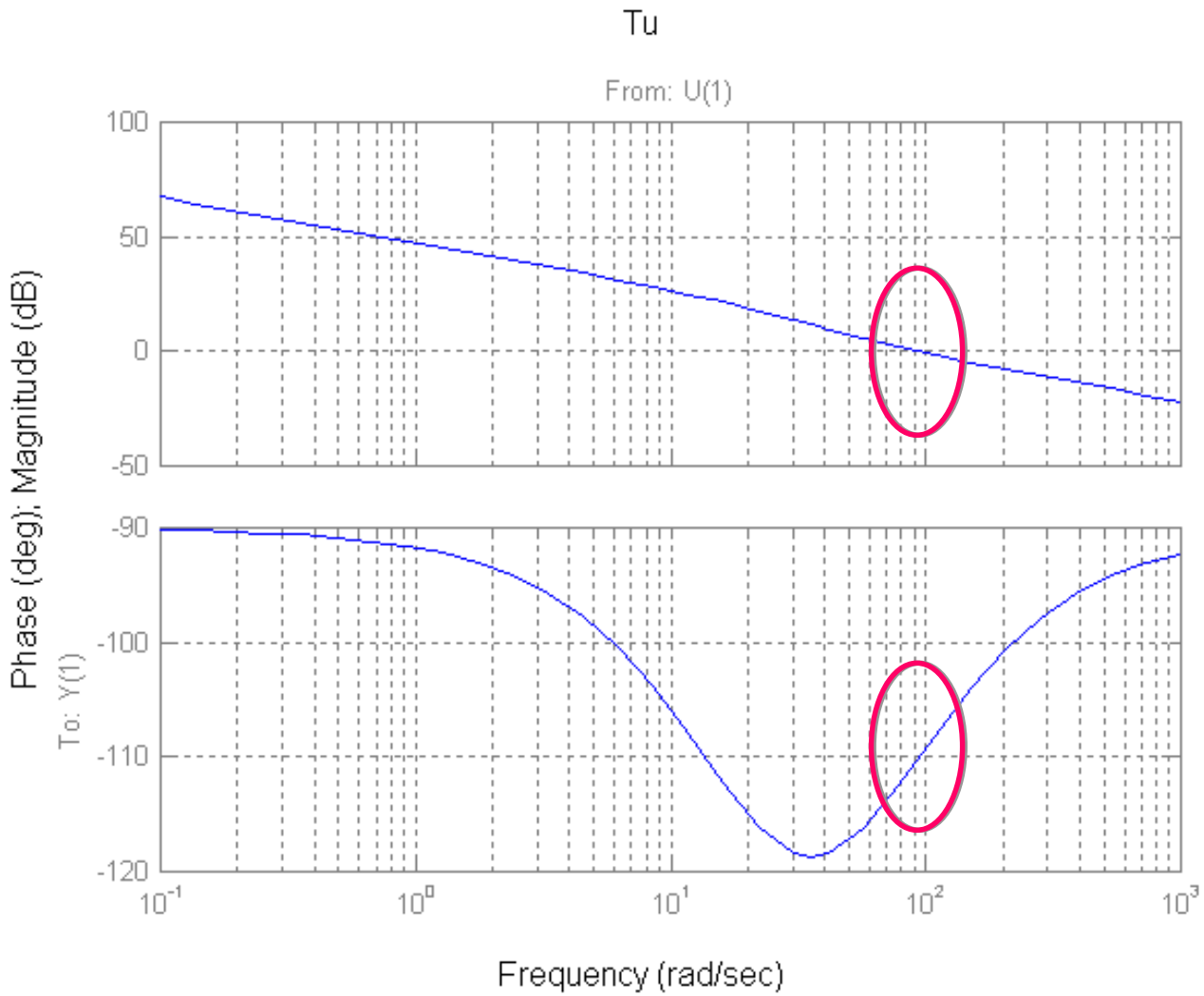


Input current control step response

DC link voltage control

- The DC link voltage control can be implemented quite straightforwardly.
- It is a simple PI regulator designed on the equivalent load resistance and DC link capacitor, as in any conventional PFC.
- The bandwidth is limited to 10 - 15 Hz to avoid input current distortion.
- Sampling frequency can be reduced accordingly. In our implementation we used 1 kHz.

DC link voltage control

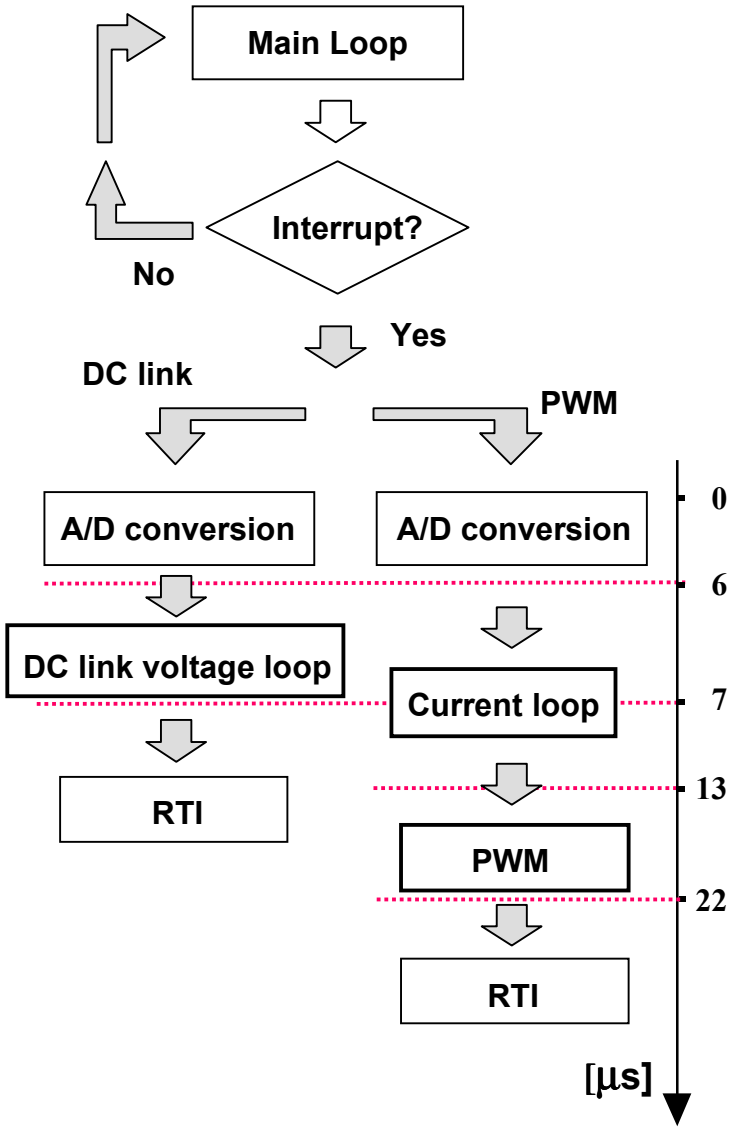


Open loop gain Bode plot.

F_{cr} = 15Hz

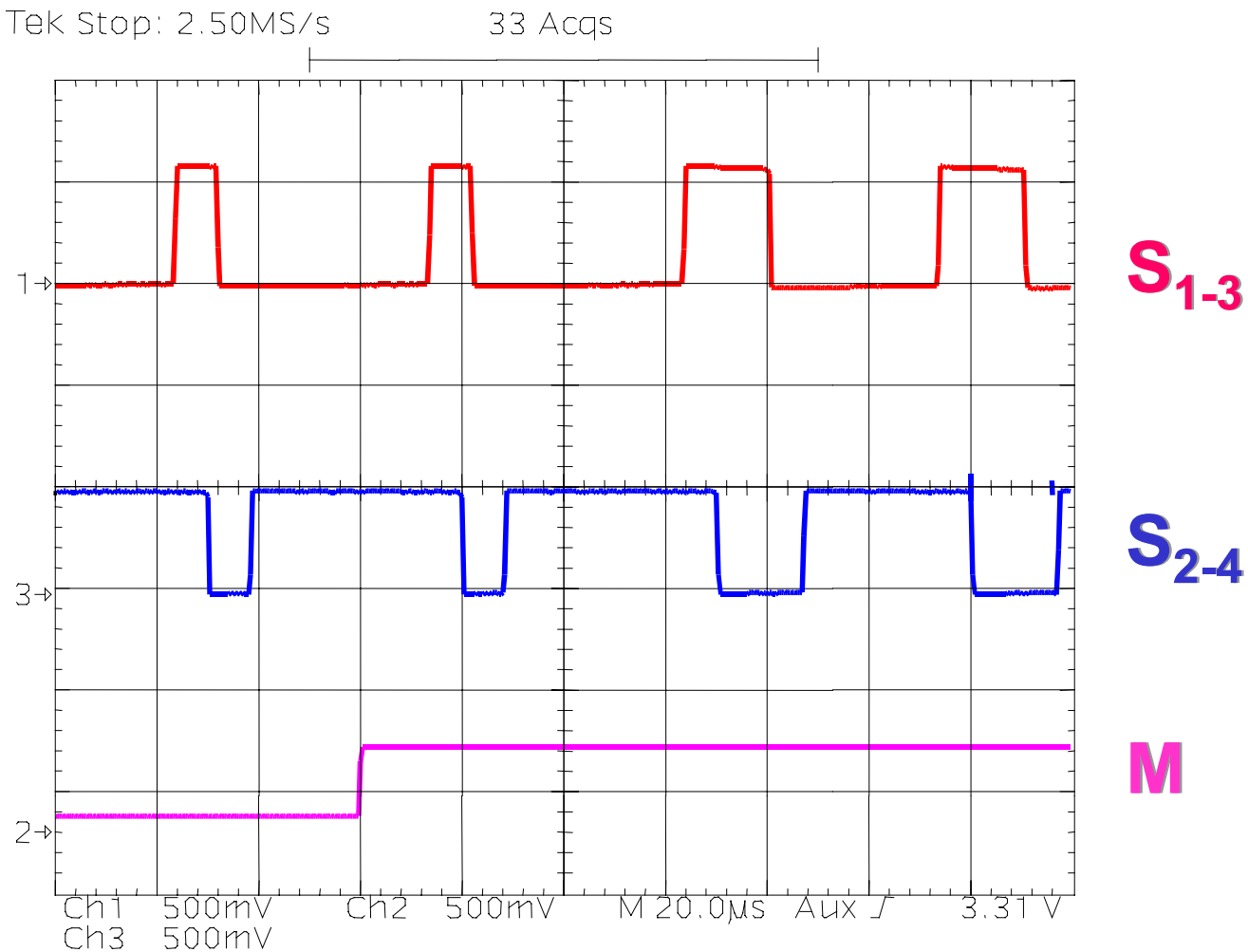
m_f = 70°

Control implementation



- The DC link voltage control routine is performed at 1 kHz sampling frequency. It requires 7 μs, including A/D conversion.
- The PWM routine, including the line current controller, is instead executed at 20 kHz. This requires 22 μs, again including A/D conversion.

PWM implementation



$S_{1\text{-}3}$

$S_{2\text{-}4}$

M

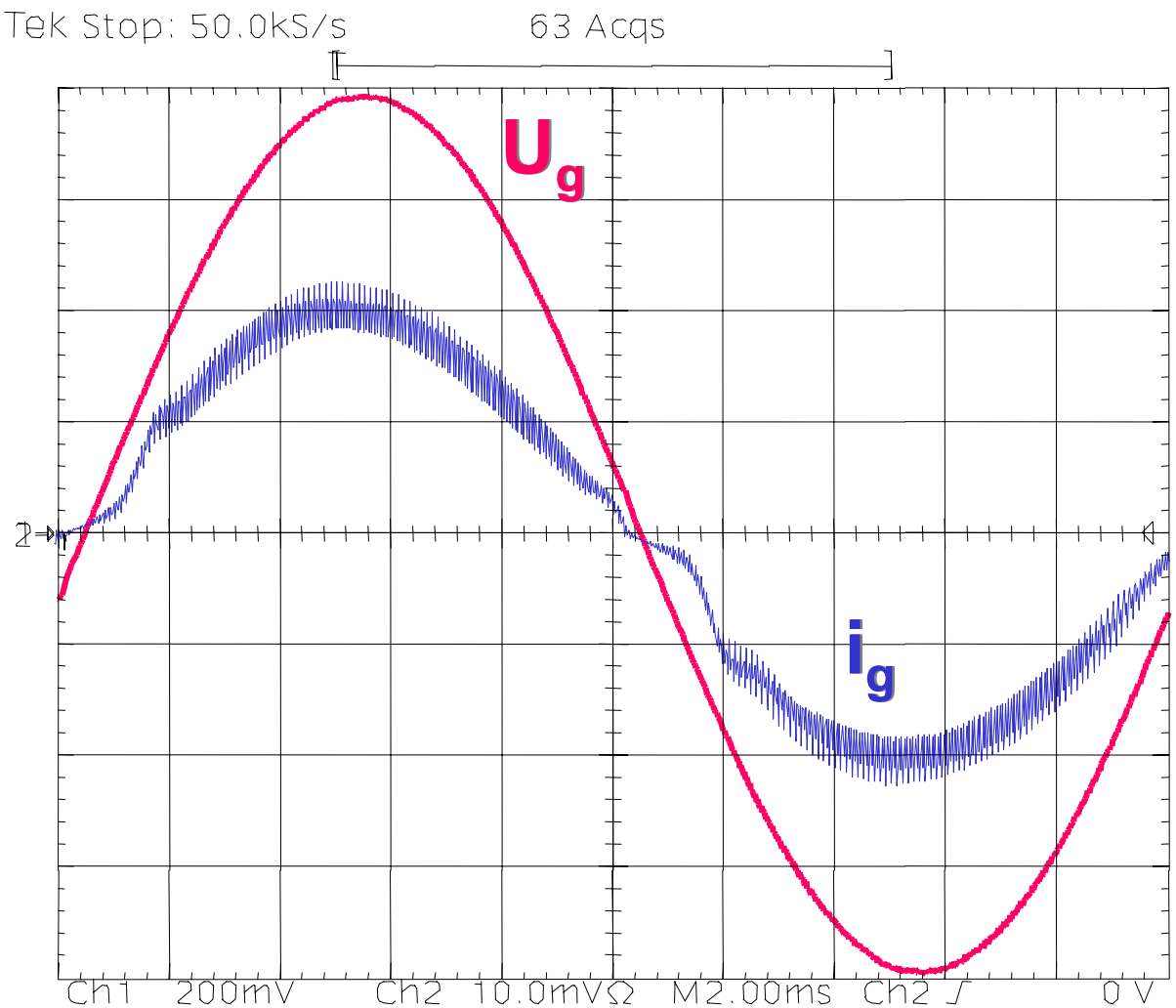
Experimental results

A prototype of the proposed converter was built to test the digital controller.

Converter Parameters

Line voltage	U_g	$110 \pm 10\%$	V_{RMS}
Output power	P_o	0.5	kW
Switching frequency	f_{sw}	20	kHz
Input inductor	L_f	1.8	mH
DC link capacitor	C_f	500	μF

Experimental results



PF = 0.98

THD = 0.15

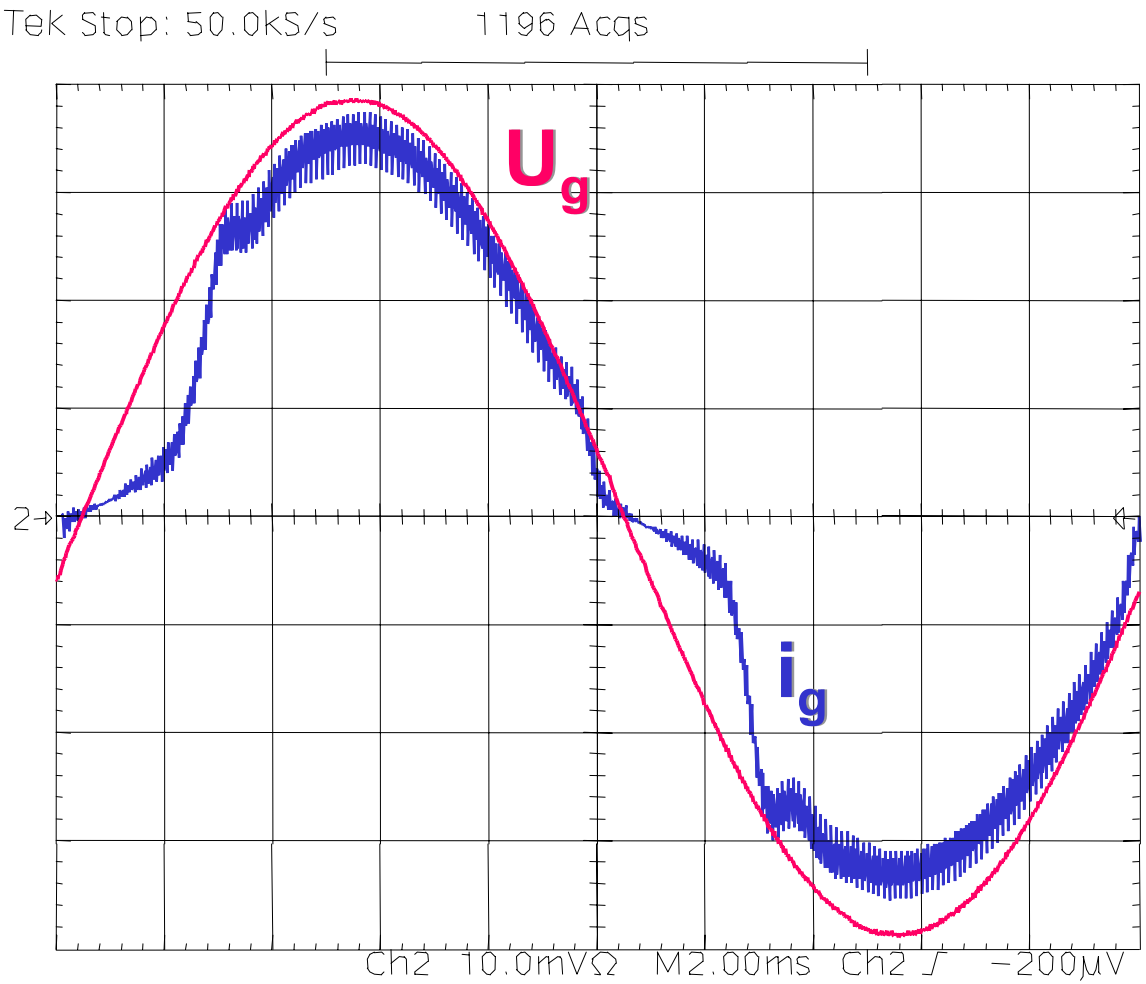
M = 0.3

P_{out} = 0.3 kW

U_g 40V/div

i_g 2A/div

Experimental results



PF = 0.96

THD = 0.35

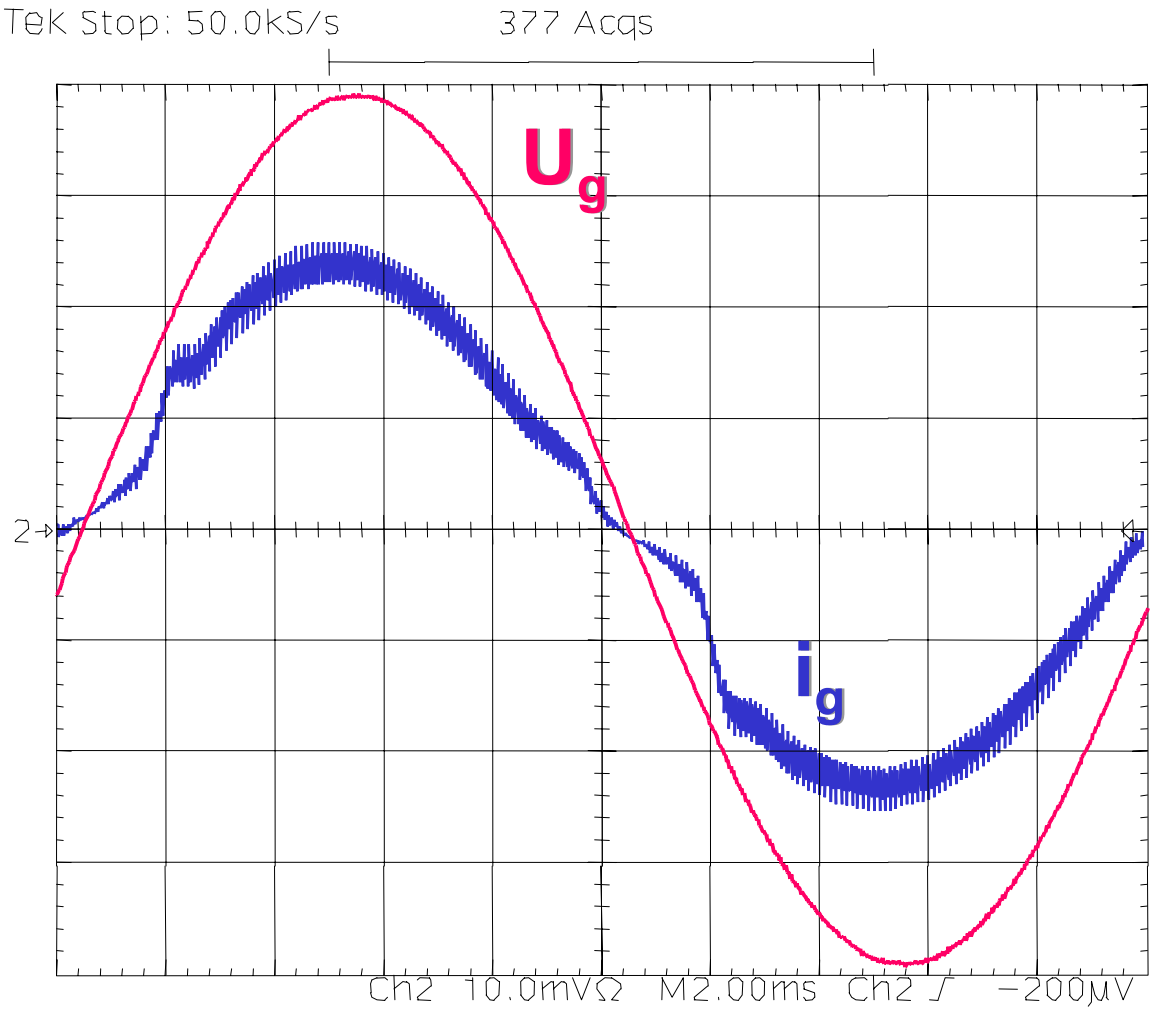
M = 0.5

P_{out} = 0.45 kW

U_g 40V/div

i_g 2A/div

Experimental results



PF = 0.97

THD = 0.25

M = 0.4

P_{out} = 0.35 kW

U_g 40V/div

i_g 2A/div

Reference

L. Rossetto, S. Buso: “Digitally-Controlled Single-Phase AC/DC Integrated PWM Converter”, IEEE IAS Annual Meeting 2001, in press.