Lesson 2

Uninterruptible Power Supply Multi-Loop Control Employing Digital Predictive Voltage and Current Regulators

Goal of the work

Investigation of digital predictive voltage and current regulators in multi-loop configuration for UPS's

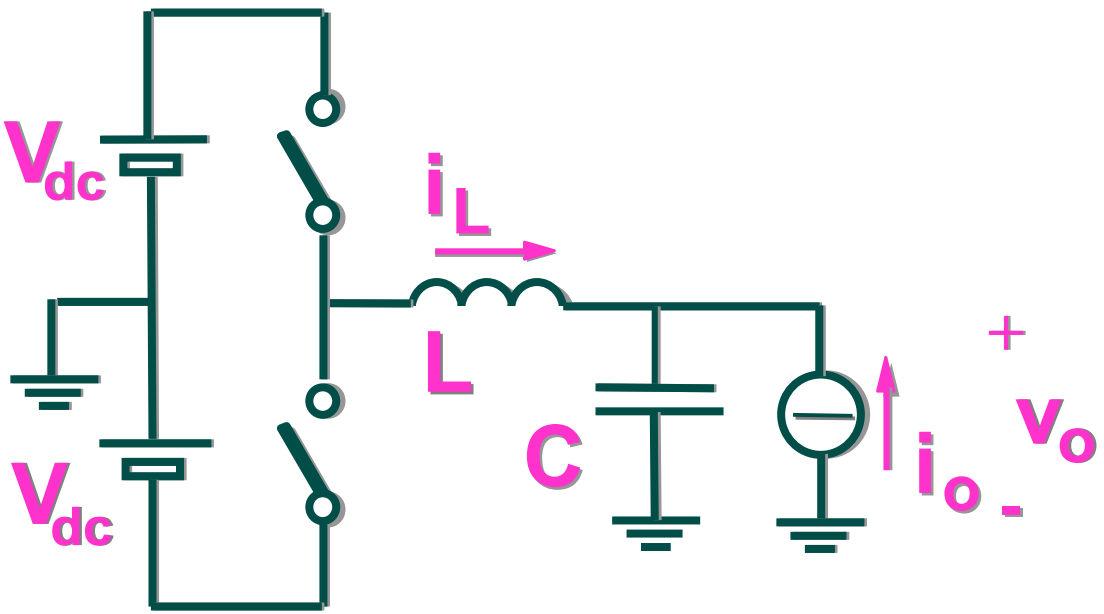
Motivations:

- **high dynamic performance (i.e. low THD with distorting loads, low overshoot under step load changes, etc…);**
- **simple control design and implementation**

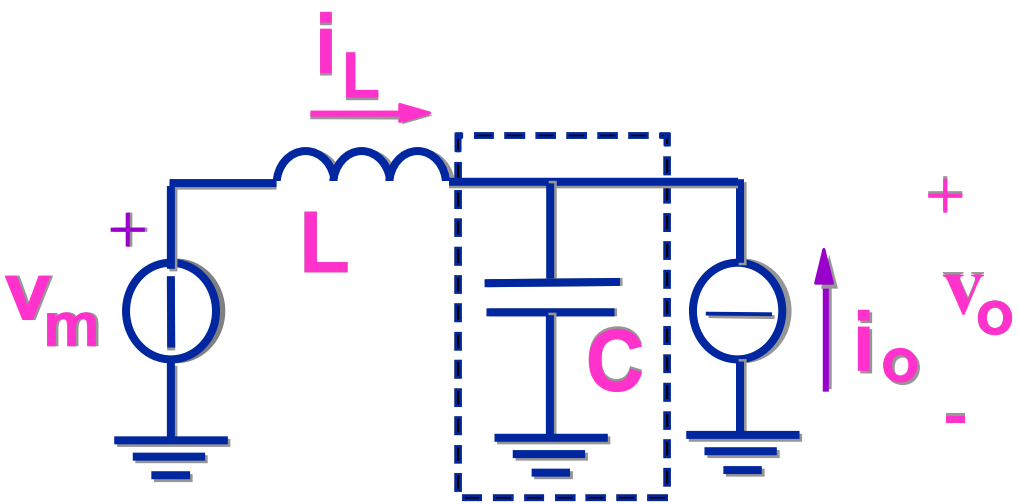
Presentation outline

- Control technique derivation:
  - current loop
  - voltage loop
- Design criteria and implementation issues
- Simulation results
- Experimental results

UPS system structure and model



Single-phase scheme



Averaged model

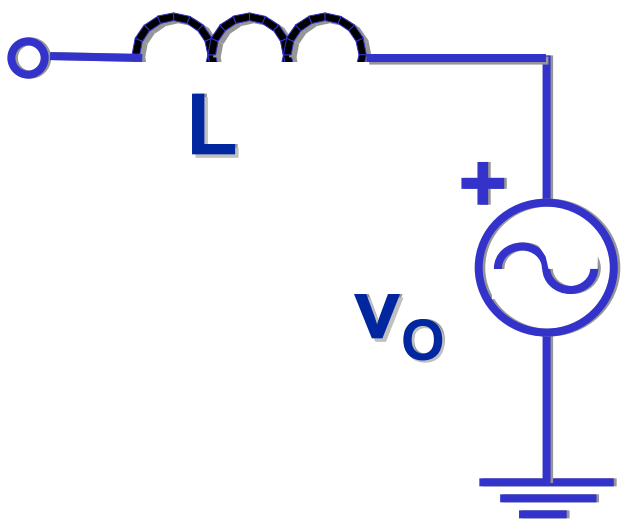
Current control loop

The control equation assumes that:

$$i_L(k+1) = i_L(k) + \frac{T_s}{L} \cdot [v(k) - v_o(k)]$$

+ one sample delay

Simple load model

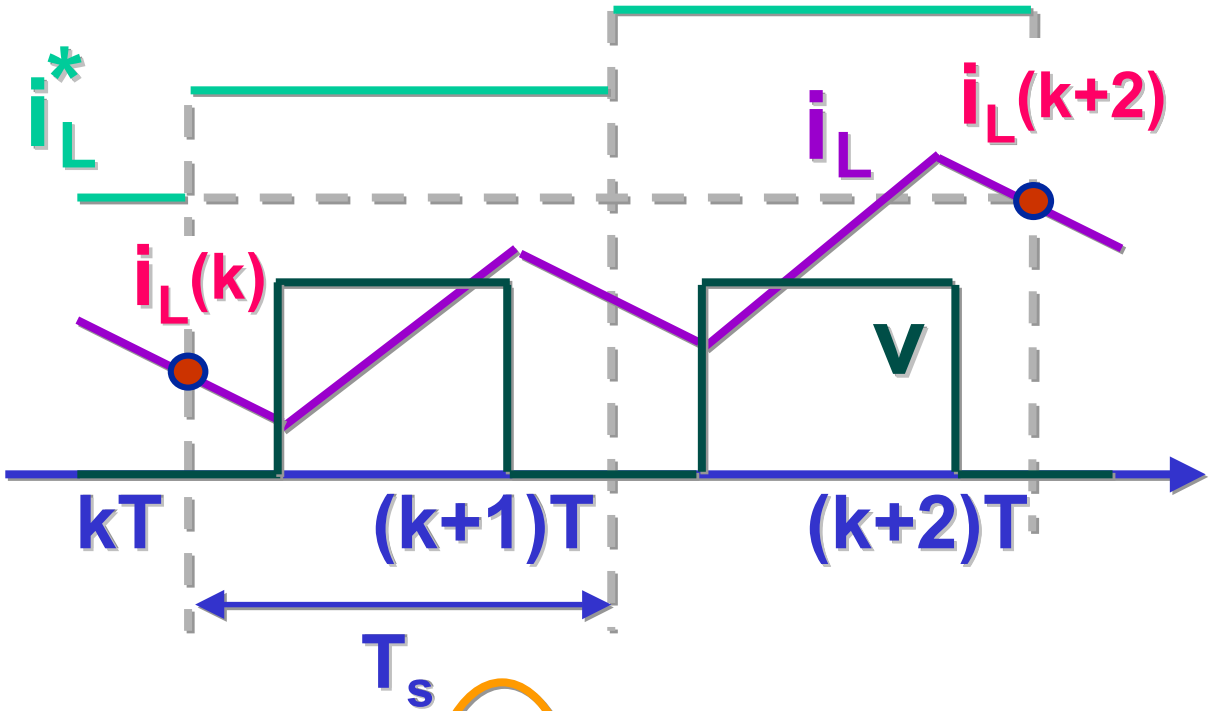


+ one sample delay

The model works properly in the UPS case if the sampling frequency is much higher (e.g. 15-20 times) than the resonance frequency of the output LC filter.

Current control loop

Review of deadbeat control



i_L^* current reference

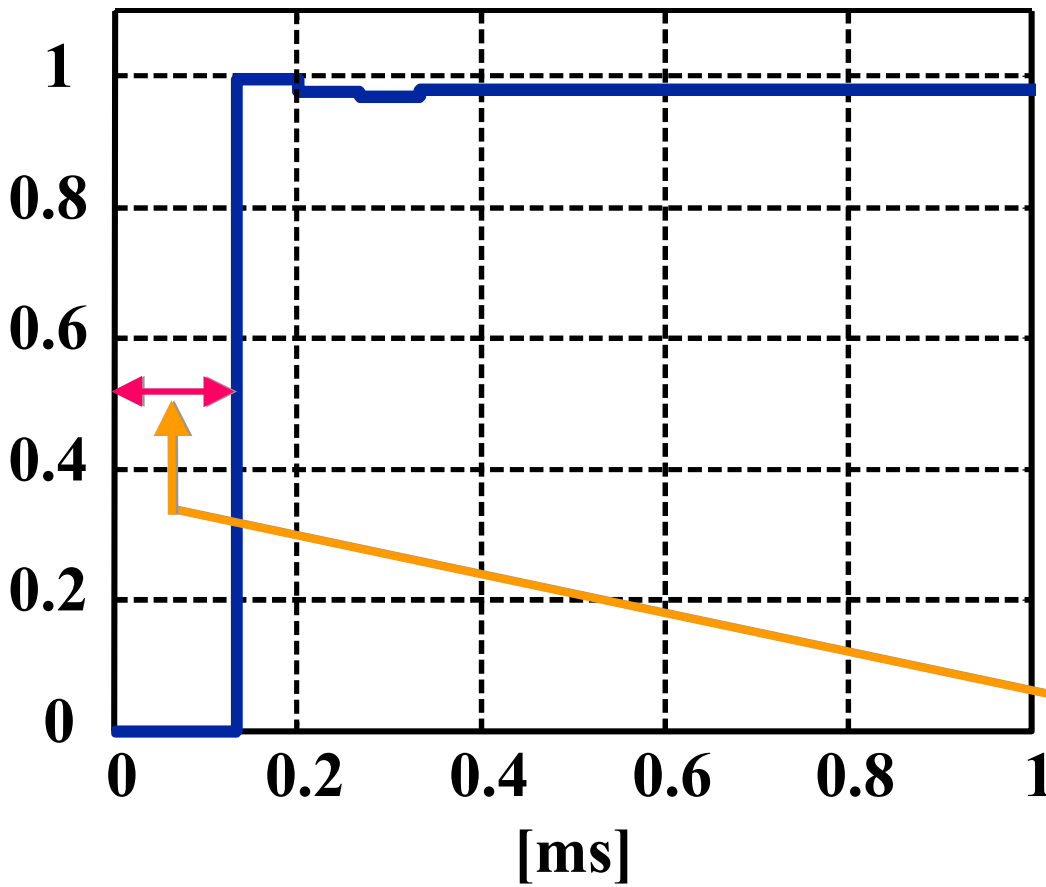
i_L inverter current

v instantaneous inverter voltage

$$v_m(k+1) = \frac{L}{T_s}\left[i_L^*(k) - i_L(k)\right] - v_m(k) + v_o(k) + v_o(k+1)$$

Dead-Beat Current Control Equation (DBCCE)

Current control loop



Step response of the closed-loop current control. Sampling frequency: 15 kHz

Two sample delay

Voltage control loop

- The same reasoning used for dead-beat current loop can be applied also to the voltage loop.
- A key point is to make the sampling period of the voltage control equal to TWICE the sampling period of the current loop.
- Thus, the current closed loop control can be modeled as a simple delay (i.e. a two sampling period delay).

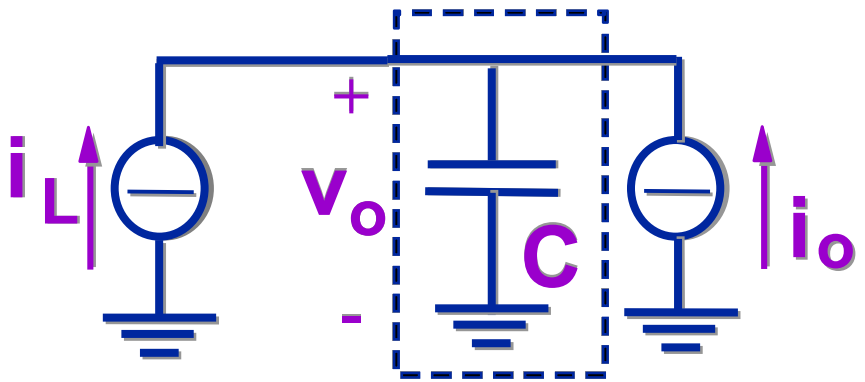
Voltage control loop

The control equation assumes that:

$$v_o(k+1) = v_o(k) + \frac{2 \cdot T_s}{C} \cdot [i_L(k) - i_o(k)]$$

+ one sample delay

Simple load model

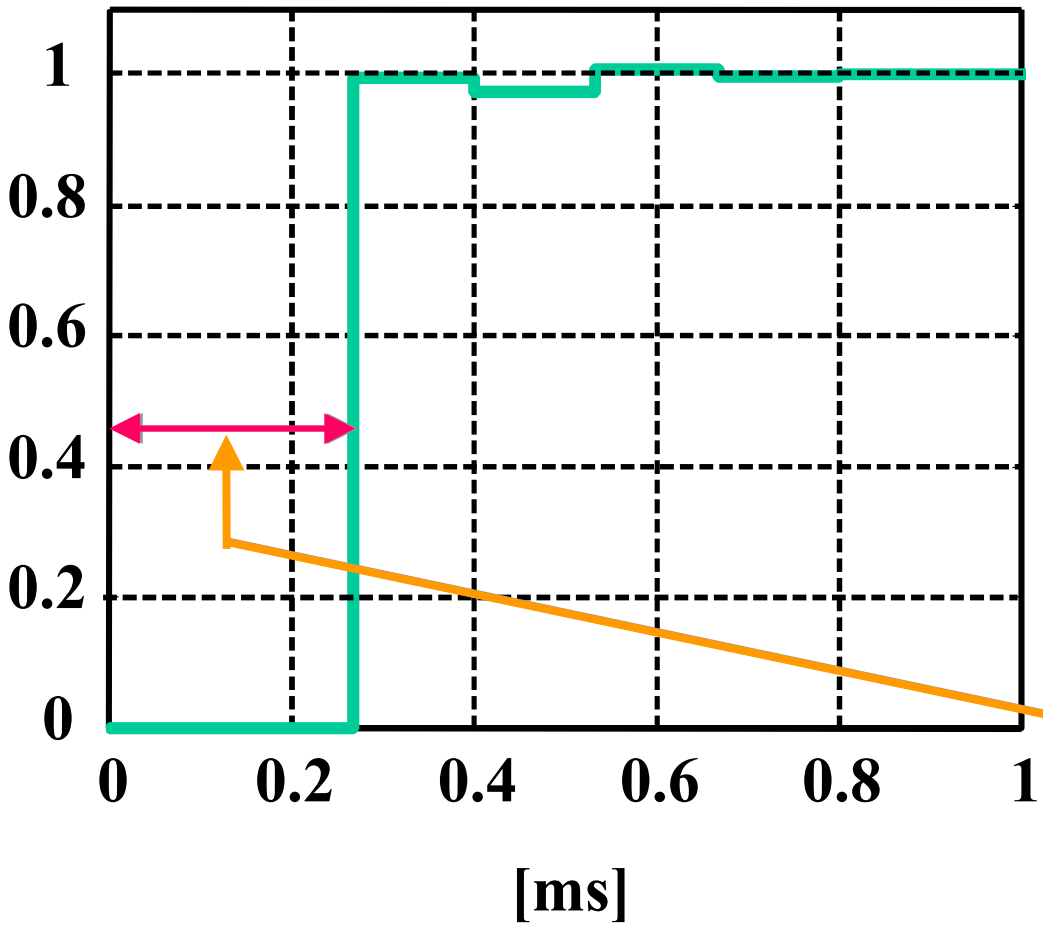


Dead-Beat Voltage Control Equation (DBVCE)

$$i_L^*(k+1) = \frac{C}{2 \cdot T_s} \cdot [v_o^*(k) - v_o(k)] - i_L(k) - i_o(k) - i_o(k+1)$$

Load current sensing

Voltage control loop



Step response of the closed-loop voltage control.

Sampling frequency: 7.5 kHz

Two sample delay

Voltage control loop
Load current estimation

- The load current does not need to be measured
- The following dead-beat (system poles in the origin) estimation is derived (DBEE):

$$\tilde{i}_o(k-1) = \frac{C}{T_s} \cdot [v_o(k) - v_o(k-1)] - i_L(k-1) \qquad (*)$$

- Estimation with system poles away from the origin implies a IIR low-pass filter on the estimated current (*)
- Practically, a moving average (FIR) filter with 4 taps was used

Voltage control loop
Control refinements

- **Feedforward of capacitor current reference**
  (obtained from output voltage reference).
- **Feedforward of the estimated load current.**
- **Interpolation between samples**
  (reduction of oscillations on inverter voltage at half of the sampling frequency).
- **Detuning of voltage control**
  (voltage estimation at instant k+1 with system pole away from the origin (low-pass filtering action) - lower sensitivity to noise).

Voltage control loop
Control refinements

Feedforward of the estimated load current (DBEE) allows the voltage dynamic equation to re-written:

$$v_o(k+1) = v_o(k) + \frac{2 \cdot T_s}{C} \cdot [i_L(k) - i_o(k)]$$

h is the index for $2T_{sw}$ sampling period

$$v_o(h+1) = v_o(h) + \frac{2T_s}{C} \cdot i_C^*(h-1)$$

Voltage control loop
Control refinements

Feedforward of also the capacitive current allows DBVCE to be re-written:

$$\Delta i_C^*(h) = \frac{C}{2 \cdot T_s} \cdot [v_o^*(h) - v_o(h)] - \Delta i_C^*(h-1)$$

Where Δi_c^* stands for the deviation of the i_c^* current from its feed-forwarded value.

Voltage control loop
Control refinements

Linear interpolation can be used to re-construct the ”missing” current sample. This modifies again the voltage dynamic equation:

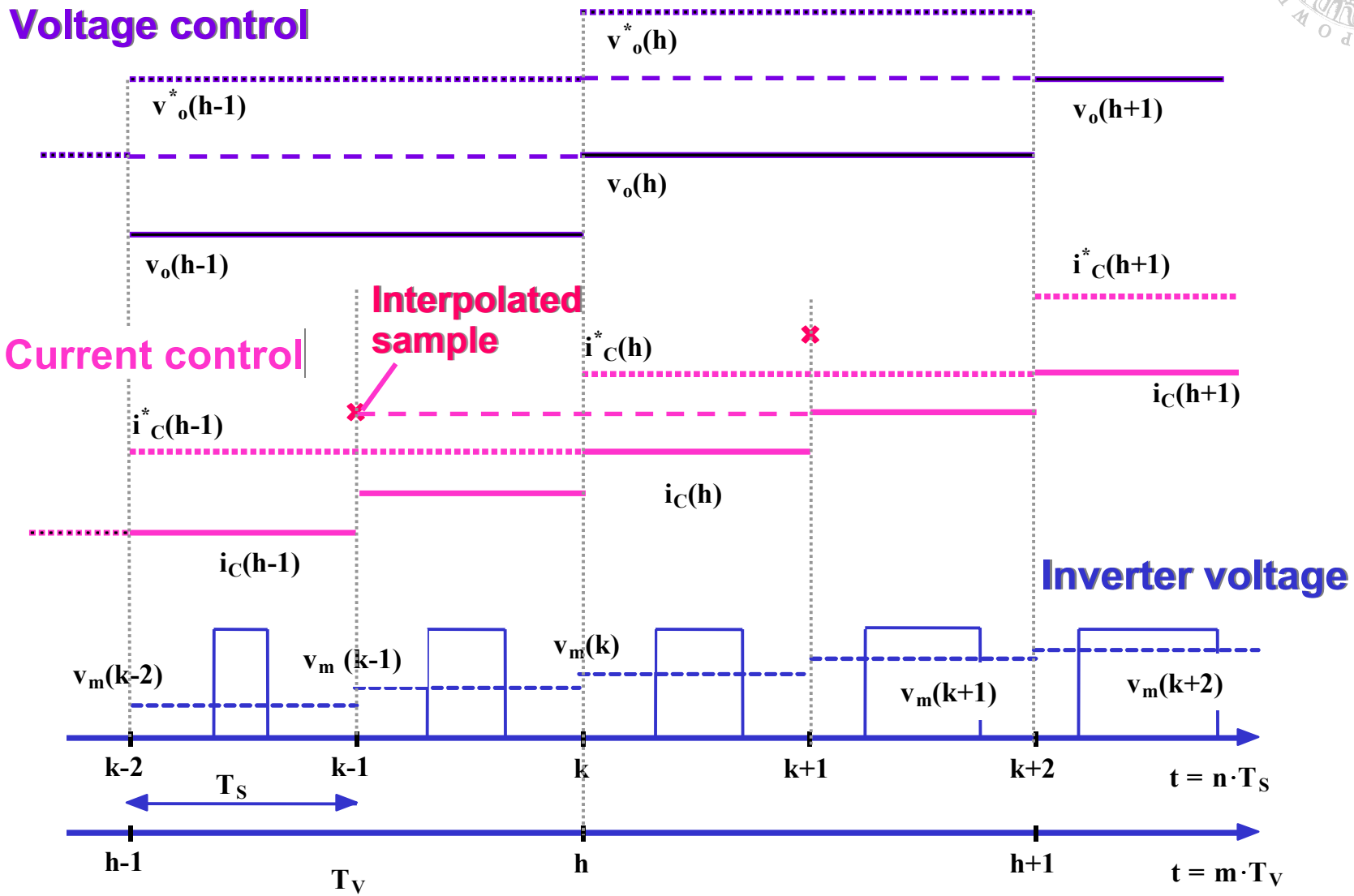
$$v_o(h+1) = v_o(h) + \frac{T_s}{C} \cdot \left[\frac{5}{2} i_C^*(h-1) - \frac{1}{2} i_C^*(h-2) \right]$$

and generates the following control equation:

$$\Delta i_C^*(h) = \frac{2}{5} \frac{C}{T_s} \cdot [v_o^*(h) - v_o(h)] - \frac{4}{5} \Delta i_C^*(h-1) + \frac{1}{5} \Delta i_C^*(h-2)$$

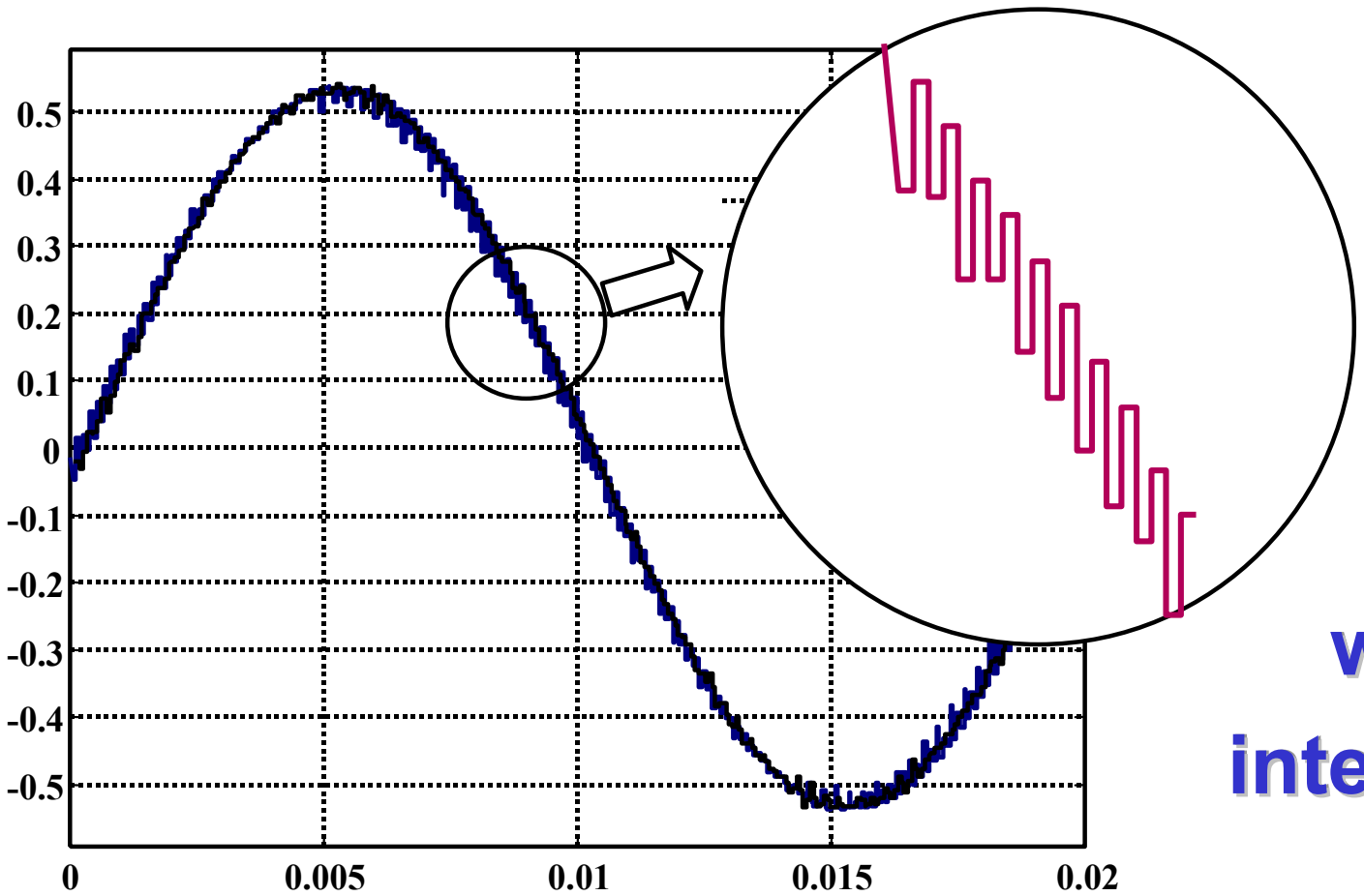
Voltage control loop

Control timing



Voltage control loop
Effects of Interpolation

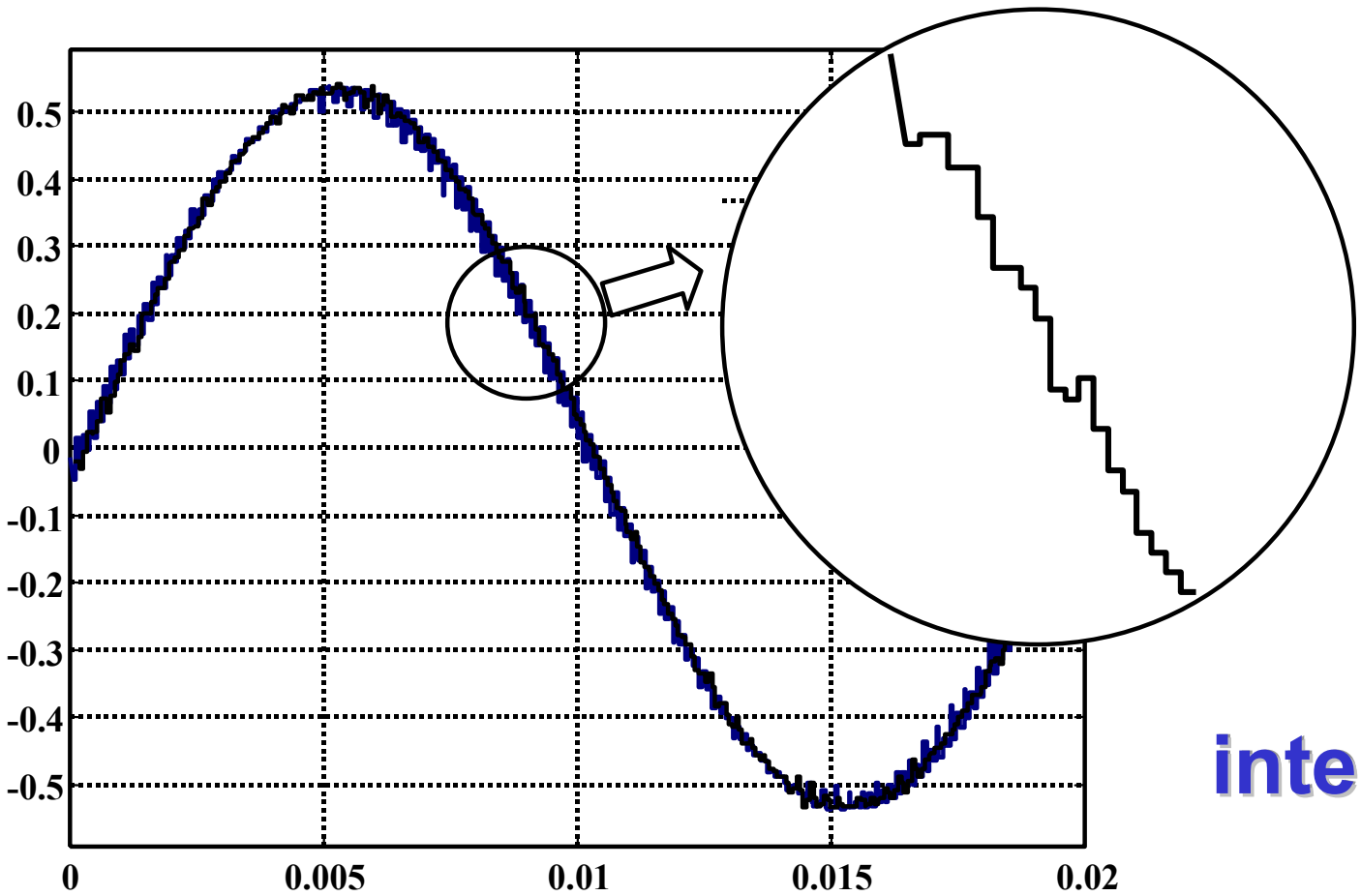
Average voltage generated by VSI



without interpolation

Voltage control loop
Effects of Interpolation

Average voltage generated by VSI

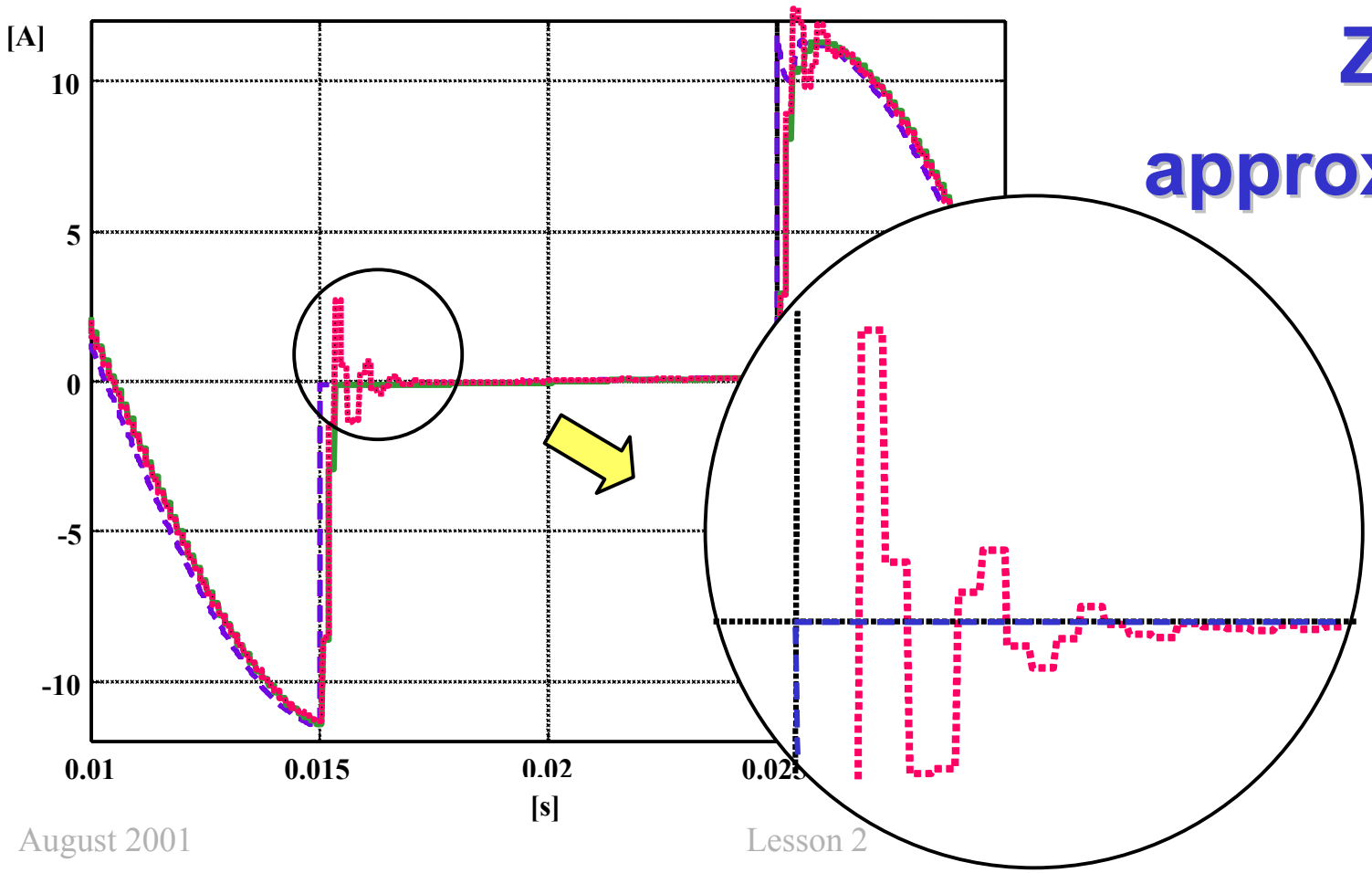


with interpolation

Voltage control loop

Load current estimation

Actual and estimated load current

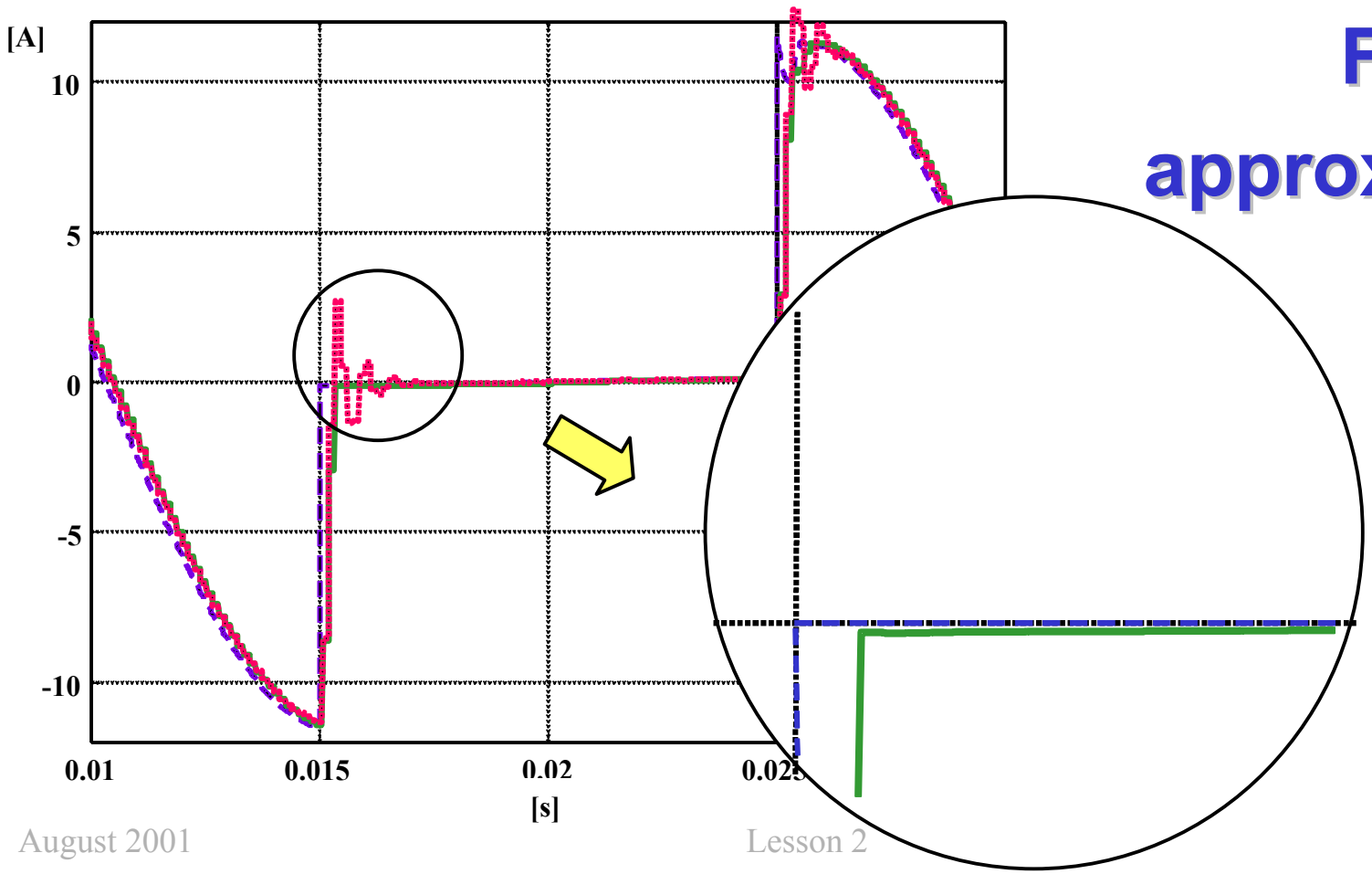


Zoh approximation

Voltage control loop

Load current estimation

Actual and estimated load current



Foh approximation

Voltage control loop
De-tuning

To improve the controller's robustness it is possible to de-tune the voltage loop. This implies the allocation of the controller pole away from the origin of the complex plane.

$$\Delta v_o(h+1) = \Delta v_o(h) + \frac{2T_s}{C} \cdot \Delta i_C^*(h-1)$$

Voltage dynamic equation for the deviations from the ideal trajectory.

Voltage control loop
De-tuning

The control law which ensures a dead-beat response is simply given by:

$$\Delta i_c^*(h) = -\frac{C}{2T_s}\Delta \hat{v}_o(h+1)$$

where $\Delta \hat{v}_o$ represents the estimated output voltage deviation (due to calculation delay we can't use the actual deviation).

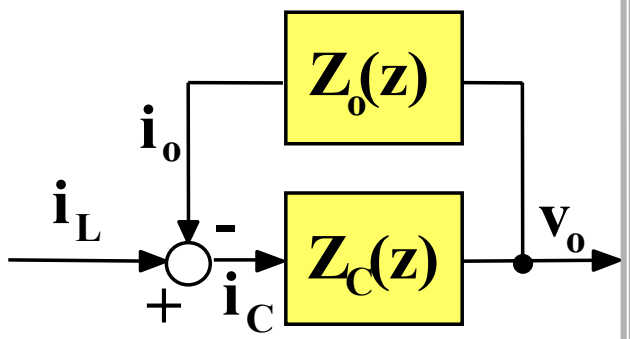
Voltage control loop
De-tuning

The estimator can have the classical Luenberger structure. K_s allows to select the pole location.

$$\Delta\hat{v}_o(h+1) = \Delta\hat{v}_o(h) + \frac{2T_s}{C}\cdot\Delta i_C^*(h-1) + K_s\left(\Delta v_o(h) - \Delta\hat{v}_o(h)\right)$$

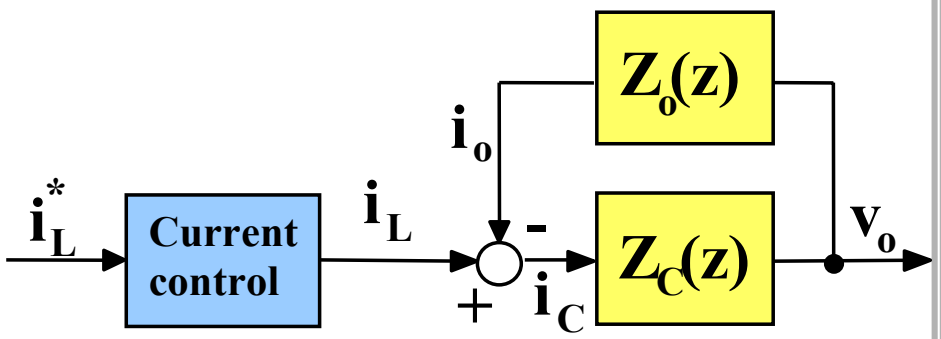
If the pole is located in the origin (dead-beat estimator) we have the usual DBVCE for the deviation. Otherwise we have a de-tuned controller with a first order response.

Control block diagram



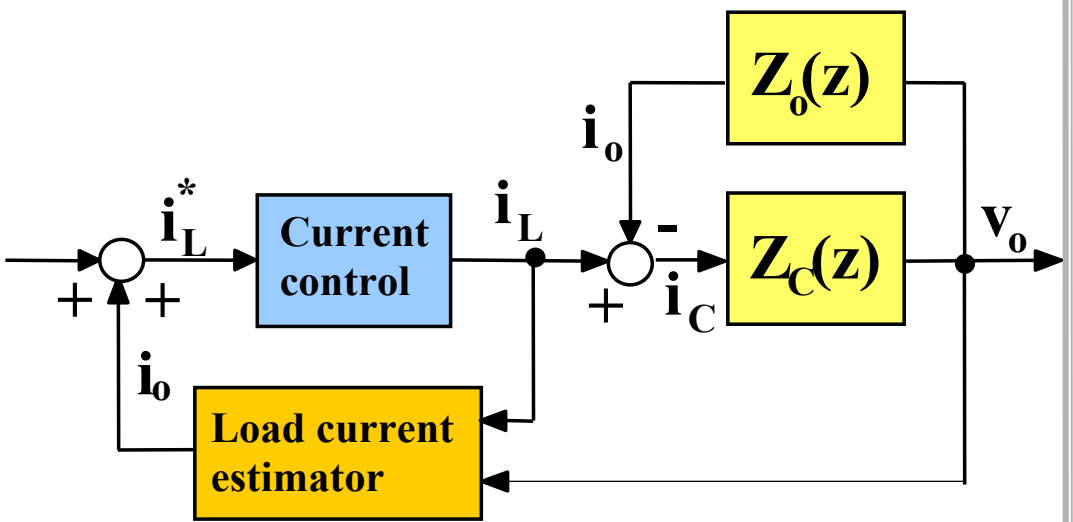
Output filter capacitor and load model

Control block diagram



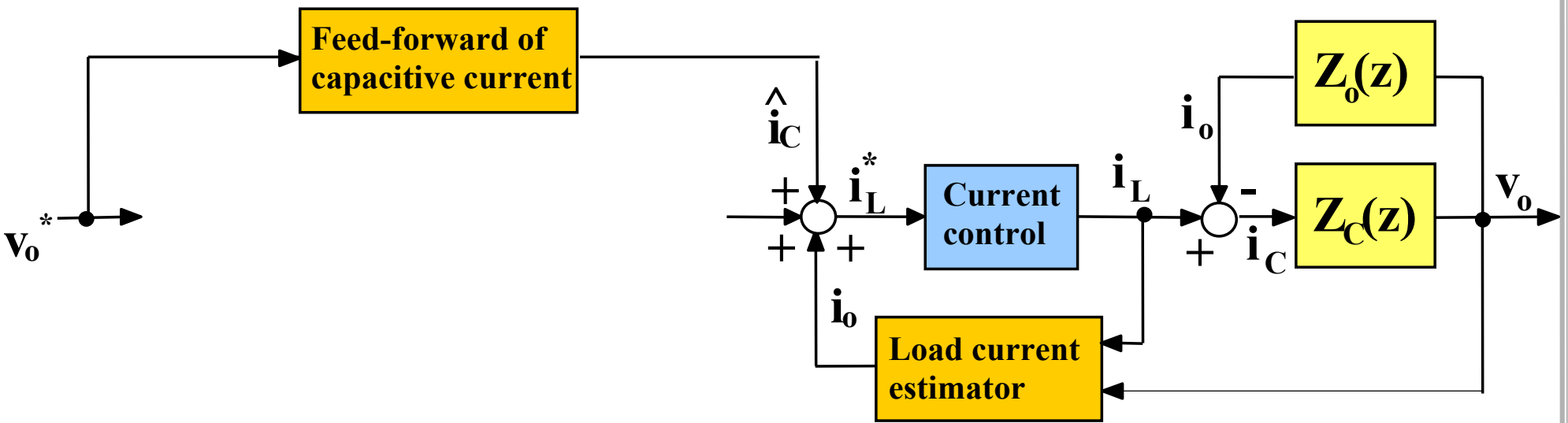
Deadbeat current control

Control block diagram



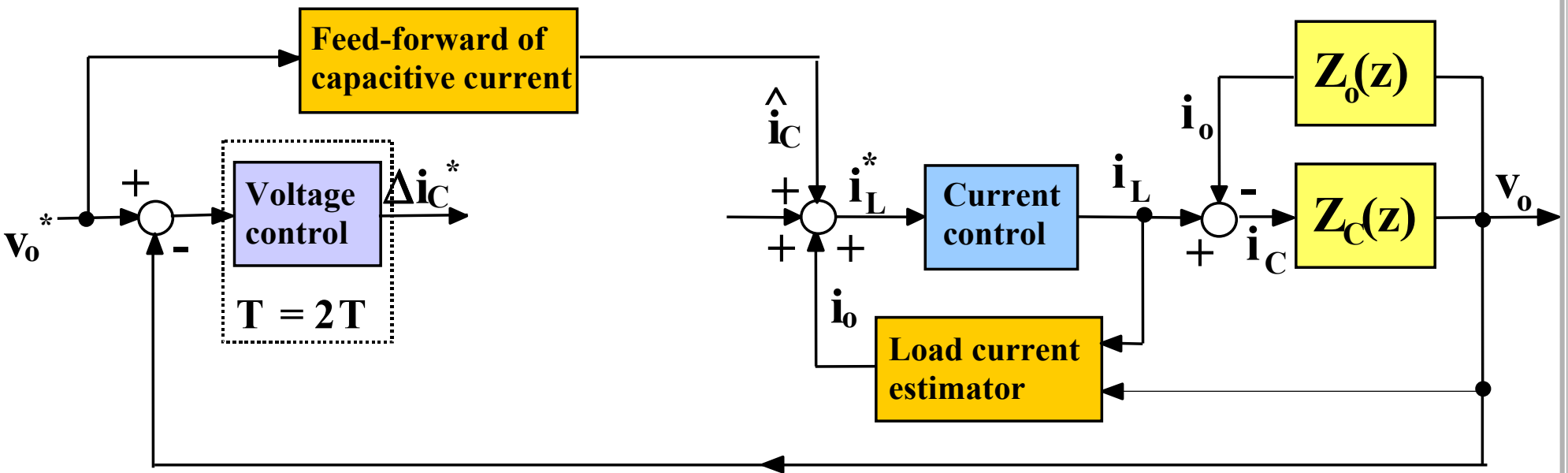
Feedforward of the estimated load current

Control block diagram



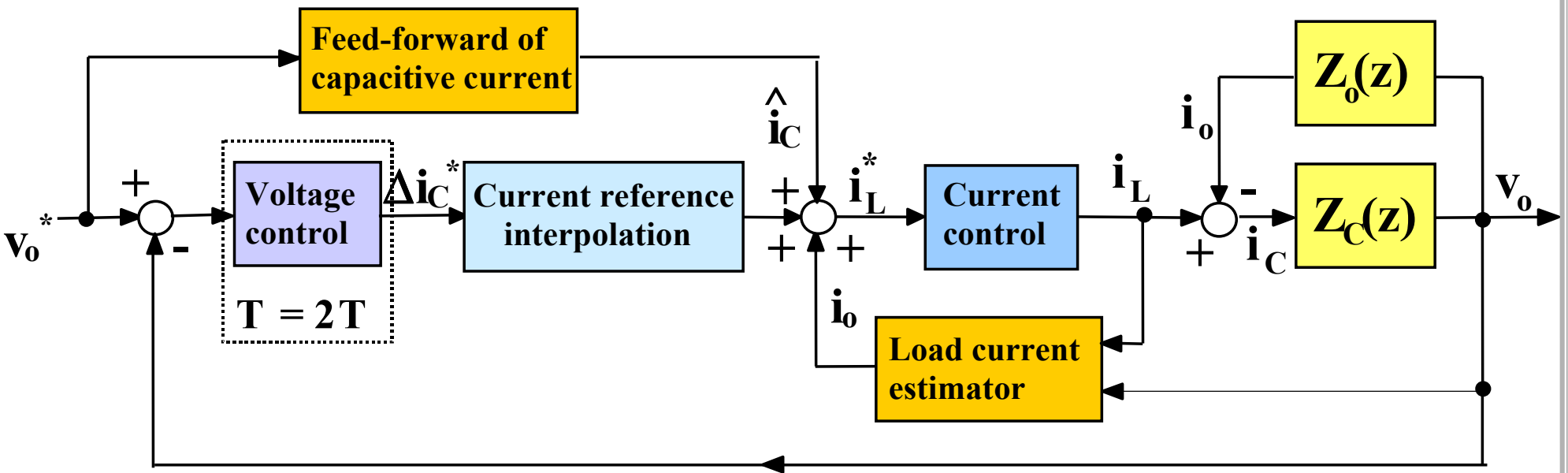
Feedforward of capacitor current reference

Control block diagram



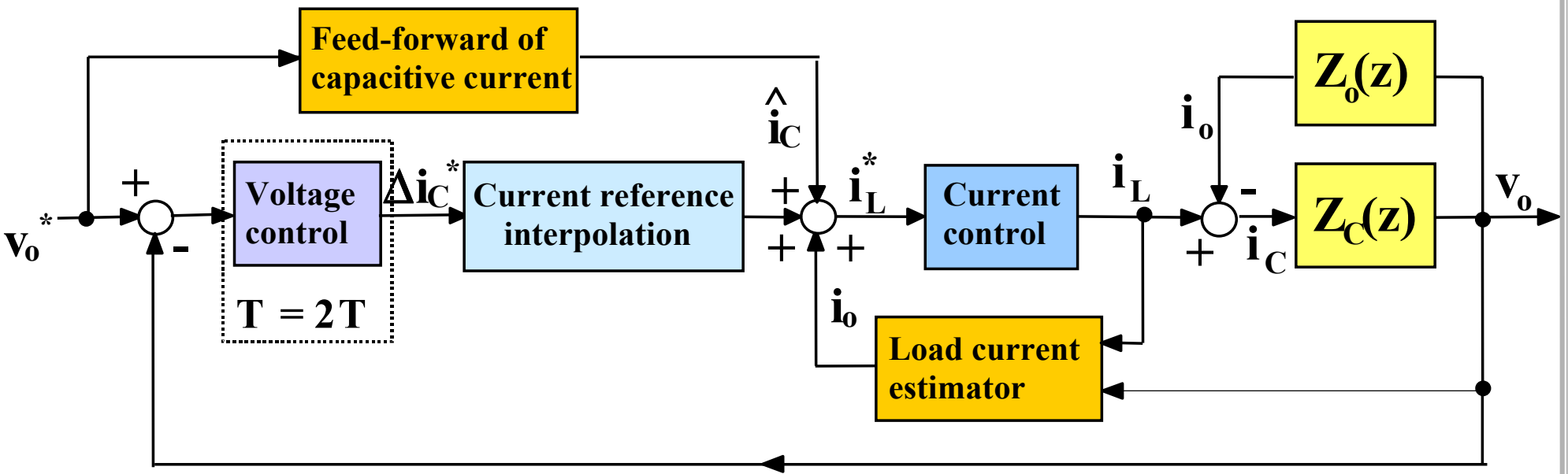
Deadbeat voltage control

Control block diagram



Capacitor current reference interpolation

Control block diagram

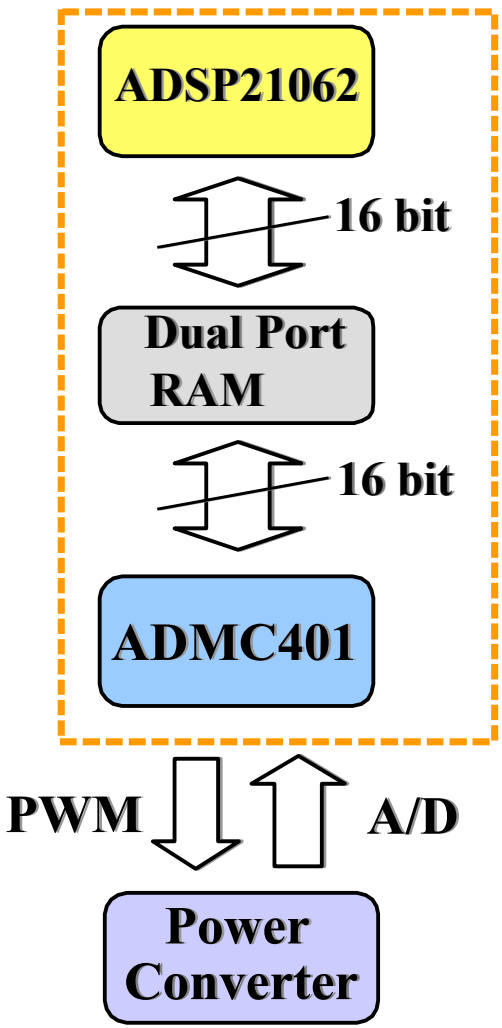


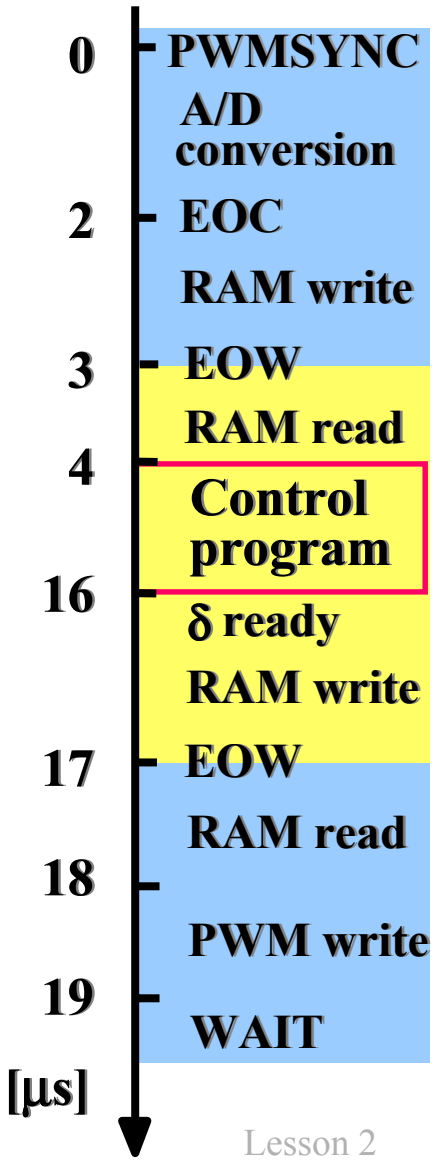
Final scheme

Control implementation

- The control program is implemented by means of a floating point DSP:
  - ADSP21062: 33 Mips, 30 ns instruction cycle
- The power converter is controlled by a motion control oriented fixed point DSP:
  - ADMC401: 26 Mips, 38.5 ns instruction cycle
- The two units are interfaced by means of a dual port RAM (1kword). A suitable communication protocol is implemented.

Control implementation



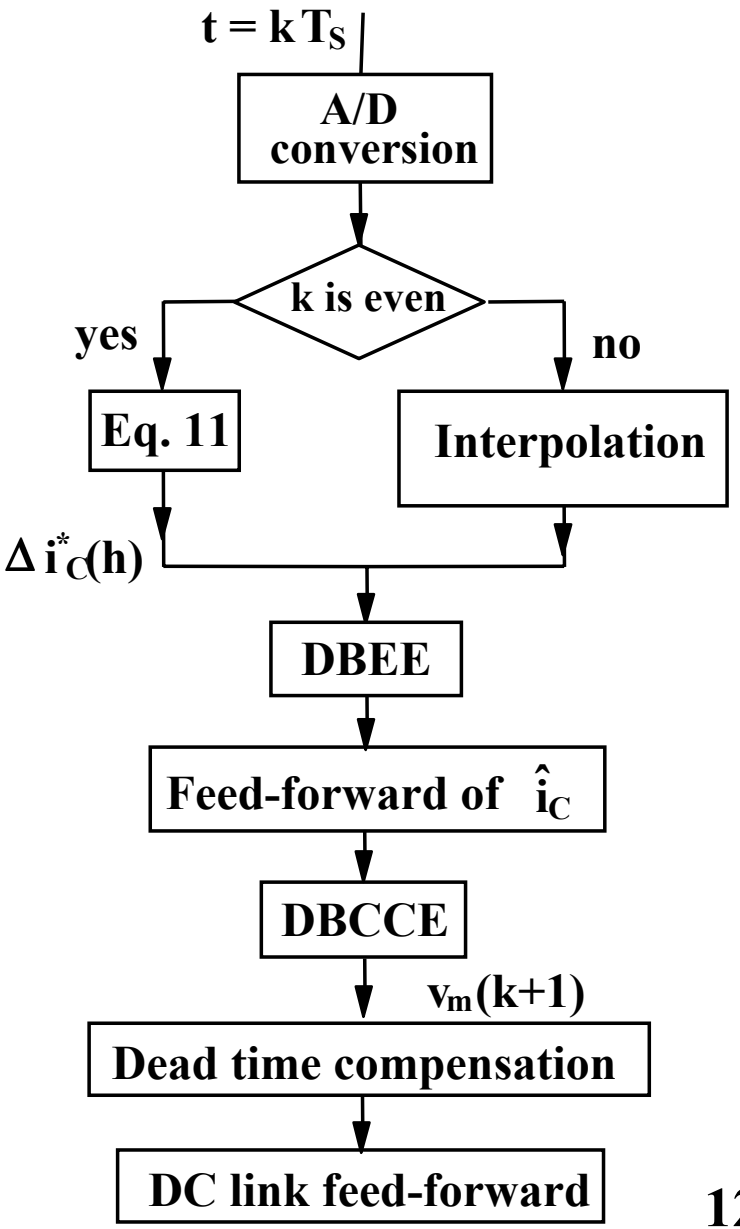


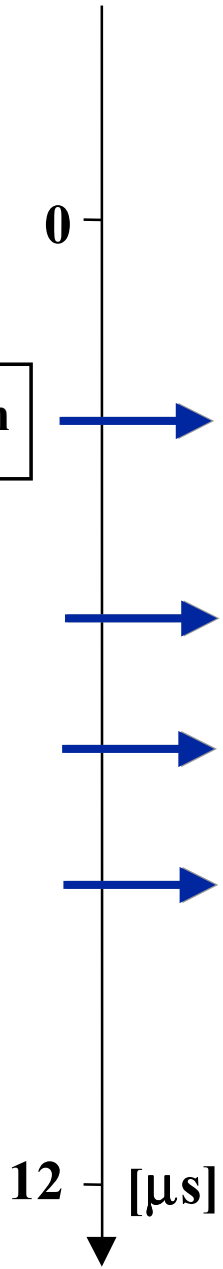
Scheme and timing of the control system

Control implementation

- The control program is written in C language, and the AD C-compiler for the ADSP 21062 is used.
- Given the very high performance of the DSP unit, no timing problem is encountered, even for very complex algorithms and 20 kHz operating frequency.
- Data exchange between the two units is dealt with by means of simple data memory write (DM) instructions.

Timing of the control algorithm





Dead-beat voltage control interpolation

Load current estimation

Capacitor current estimation

Dead-beat current control

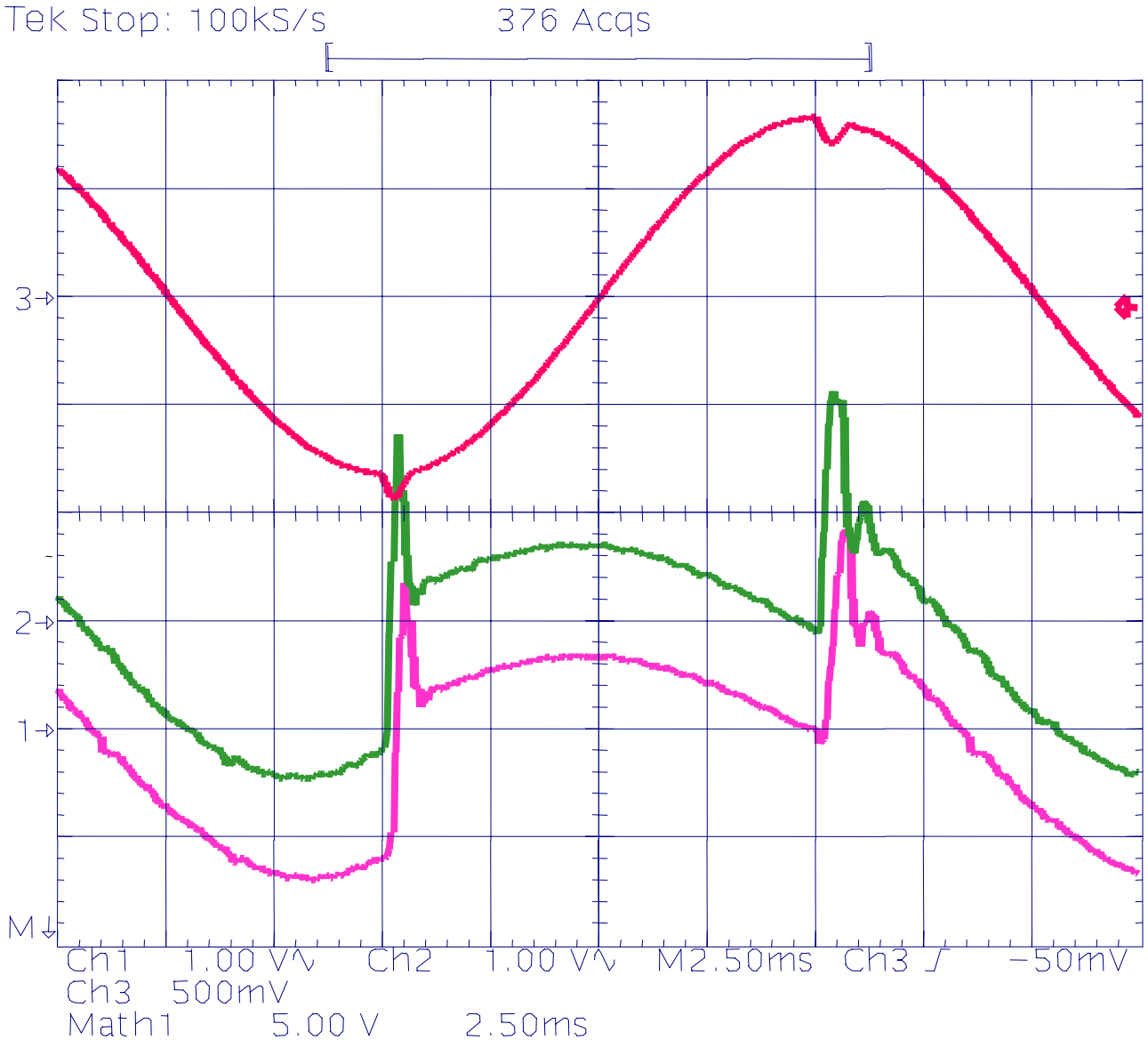
50% increase compared to PI control

Experimental results

Experimental prototype's parameters

Nominal output power	P_o	1	[kVA]
Nominal output voltage	V_{oRMS}	115	[V]
Minimum load DF	$\cos\phi$	0.8	
DC link voltage	V_{DC}	250	[V]
Output frequency	f_o	50	[Hz]
Output inductor	L	1.8	[mH]
Output capacitor	C	120	[μF]
Switching frequency	f_s	15	[kHz]

Experimental results



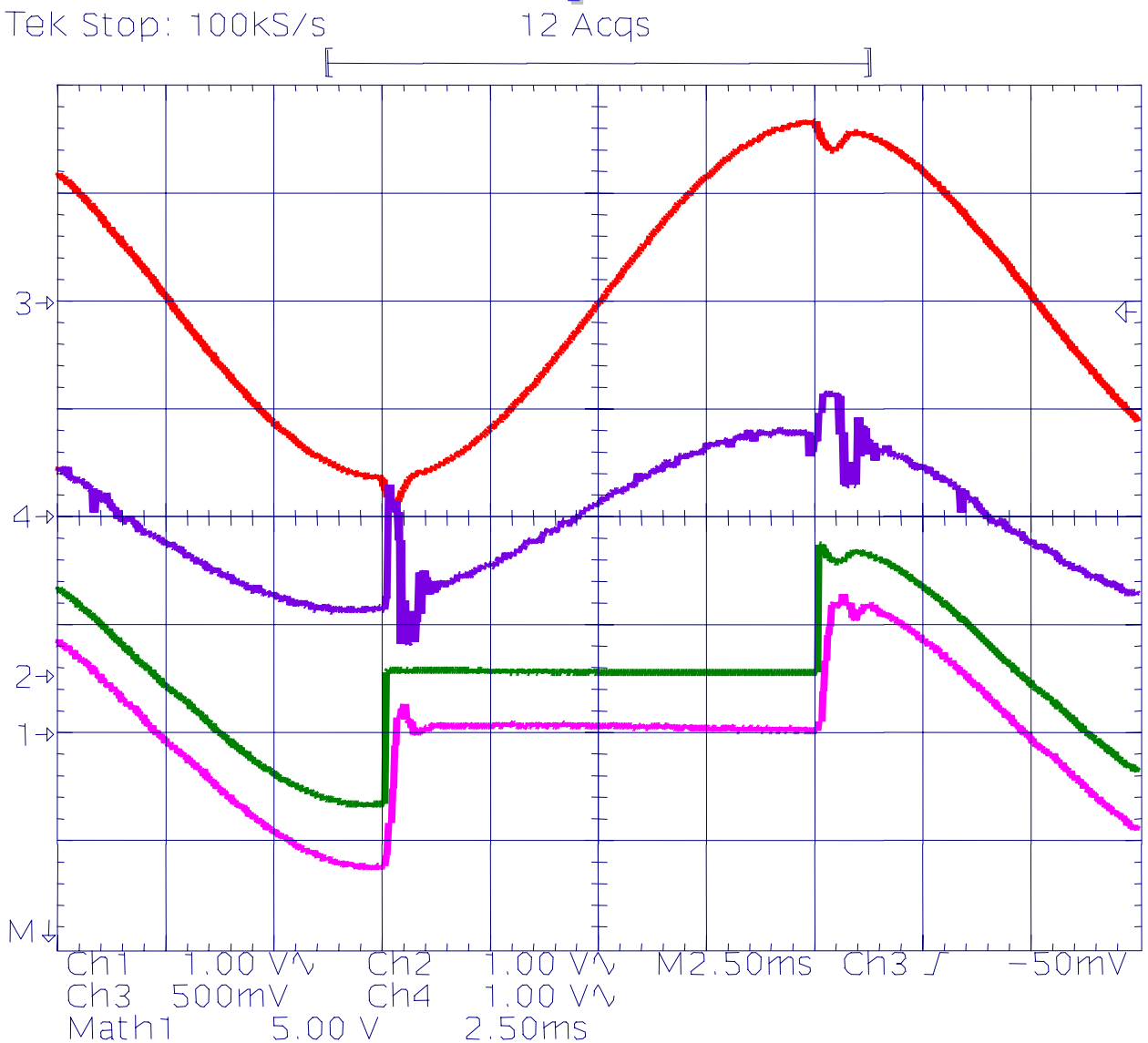
Step load variations 100% - 0%

Output voltage [100V/div]

Current reference [10A/div]

Actual current [10A/div]

Experimental results



Step load variations 100% - 0%

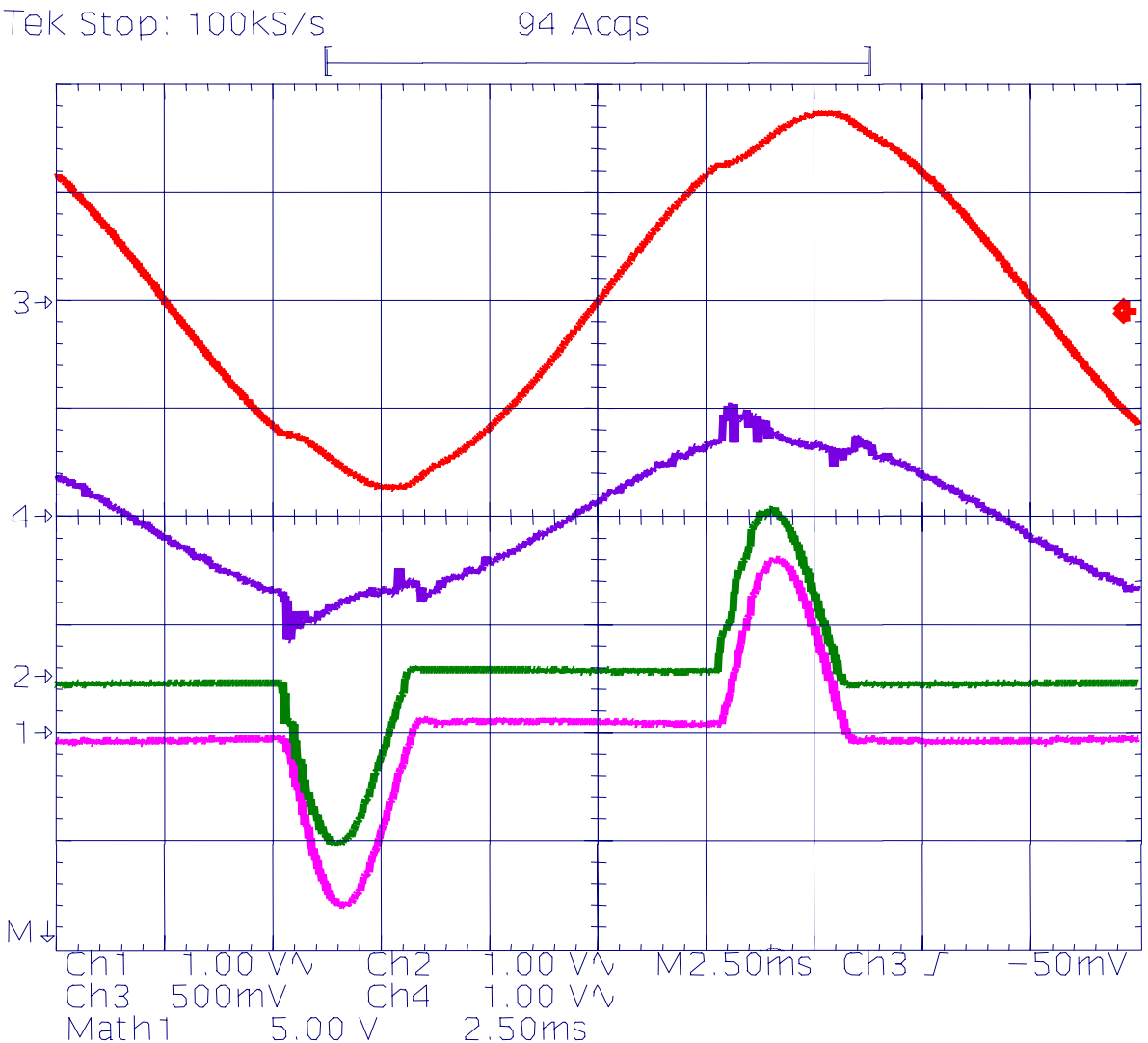
Output voltage [100V/div]

Reference voltage [200V/div]

Load current [10A/div]

Estimated current [10A/div]

Experimental results



THD=3.4%

Distorting load

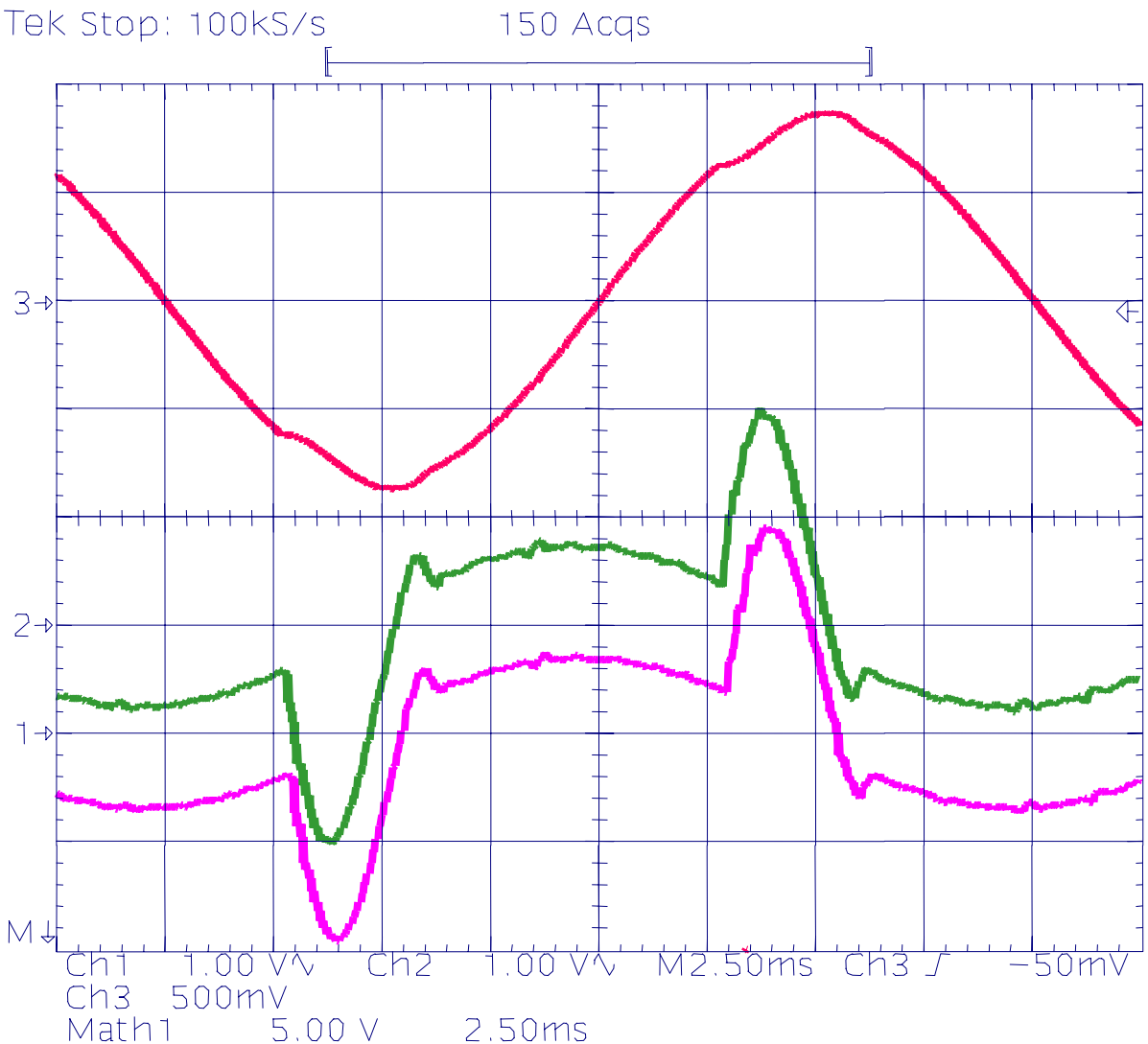
Output voltage [100V/div]

Reference voltage [200V/div]

Load current [10A/div]

Estimated current [10A/div]

Experimental results



Distorting load

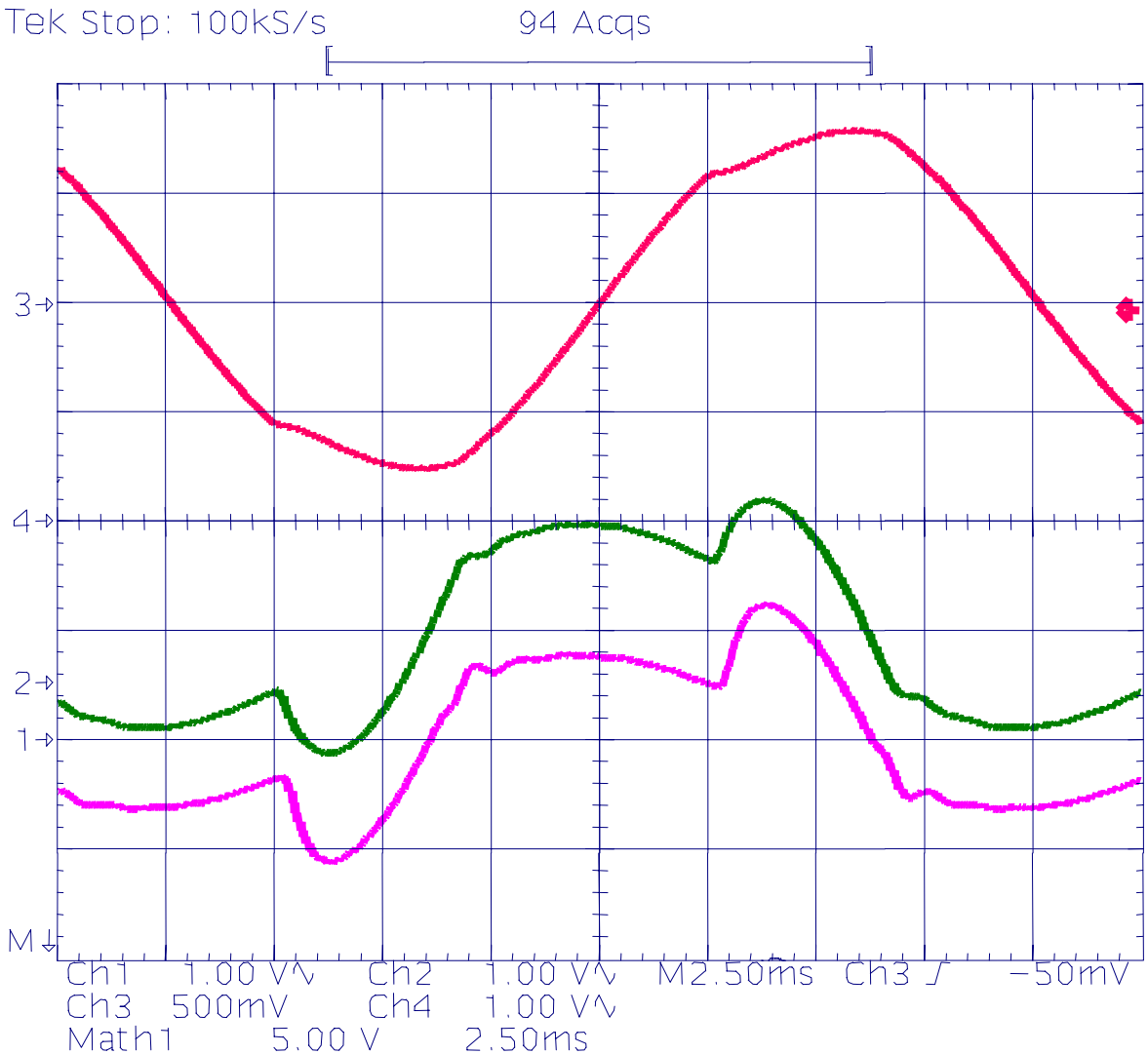
Output voltage [100V/div]

Current reference [10A/div]

Actual current [10A/div]

THD=3.4%

Experimental results



THD=6.0%

Distorting load
PI control

Output voltage [100V/div]

Current reference [10A/div]

Actual current [10A/div]

Reference

S. Buso, S.Fasolo, P. Mattavelli, "Uninterruptible Power Supply Multi-Loop Control Employing Digital Predictive Voltage and Current Regulators", Applied Power Electronics Conference (APEC) Proc., Anaheim, California, 4-8 March, 2001, pp. 907-913.