Fundamental Definitions

Electromagnetic Compatibility

- The capability of electrical and electronic systems, equipment, and devices to operate in their intended electromagnetic environment within a defined margin of safety, and at design levels of performance, without suffering or causing unacceptable degradation as a result of electromagnetic interference

Fundamental Definitions

Electromagnetic Interference (EMI)

- EMI is the process by which disruptive electromagnetic energy is transmitted from one elctronic device to another via radiated and/or conducted paths. In common usage, EMI refers particularly to RF signals, but it can occur in any frequency range starting from DC

Fundamental Definitions

Susceptibility

- A relative measure of a device or a system's propensity to be disrupted or damaged by EMI exposure to an incident field of signal. It is the lack of immunity

Immunity

- A relative measure of a device or system's ability to withstand EMI exposure while maintaining a predefined performance level

Fundamental Definitions

Radiated Immunity

- A Product's relative ability to withstand electromagnetic energy that arrives via free-space propagation

Conducted Immunity

- A Product's relative ability to withstand electromagnetic energy that penetrates it through external cables, power cords, and I/O interconnects

Fundamental Definitions

Electrostatic Discharge (ESD)

- A transfer of electric charge between bodies of different electrostatic potential in proximity or through direct contact. The term ESD is generally applyed to events that are triggered by human beings

Fundamental Definitions

Containment

- A process whereby RF energy is prevented from exiting an enclosure, generally by shielding a product within a metal enclosure. Reciprocally, we can also speak of containment as preventing RF energy from entering the enclosure

Fundamental Definitions

Suppression

- The process of reducing or eliminating RF energy that exists without relying on a secondary method, such as a metal housing or chassis. Suppression may include shielding and filtering as well

EMI Transmission Path

Interference can be reduced acting on:

- Source (layout, filtering, shielding)
- Channel (layout)
- Receiver (layout, filtering, shielding)

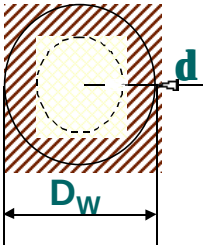
NOTE: EMI is most economically soppressed at the source in the design phase

Relevant EMI "Components"

- Only one third of the components affecting EMI are on the schematics
- Another third are parasitic elements within components
- The final third are created by PC board trace routing, and component mounting, placement, and even orientation

Resistivity of a Cylindric Conductor

DC: $r_{BF} = \frac{4}{\pi D_W^2} \quad [\Omega / m]$



AC: $\delta = \sqrt{\frac{1}{\pi \sigma \mu f}}$ Skin depth (σ = conducibility)

$$r_{AF} @ \frac{1}{\delta} \sqrt{\frac{\mu}{\sigma}} \sqrt{f} \quad [\Omega / m]$$

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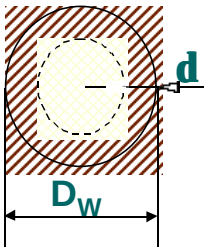
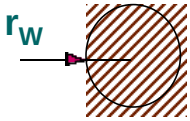


AC: $\delta = \frac{1}{\sqrt{\mu_o \sigma \pi f}}$ Skin depth (σ = conducibility)

$$r_{AF} \approx \frac{1}{D_W}\sqrt{\frac{\mu_o}{\pi\sigma}}\sqrt{f} \quad [\Omega / m]$$

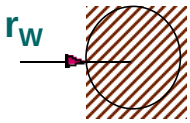
Internal and External Inductances



$$\ell_i \approx \frac{1}{4\pi r_W}\sqrt{\frac{\mu_o}{\pi\sigma}}\frac{1}{\sqrt{f}} \quad [H / m]$$

$$\ell_e \approx \frac{\mu_o}{\pi} \operatorname{acosh}\left(\frac{s}{2r_W}\right) \quad [H / m]$$

Internal and External Inductances



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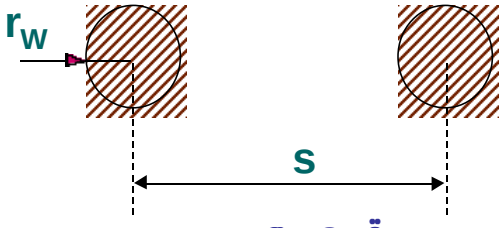
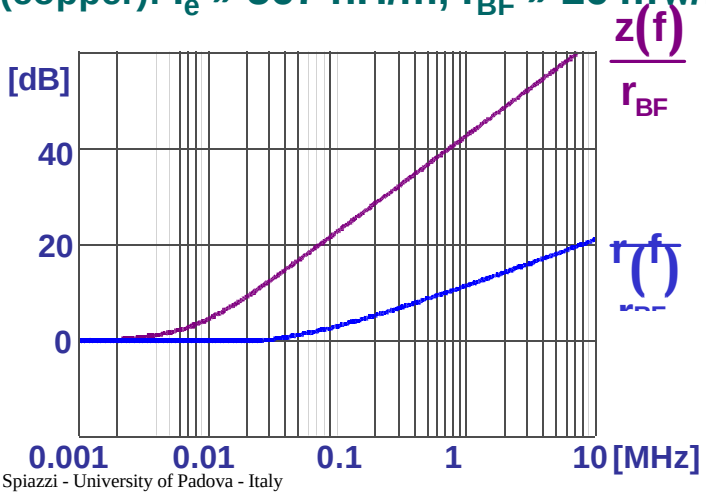


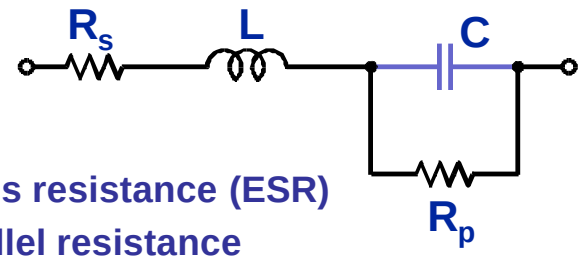
$$\ell_e \approx \frac{\mu_o}{\pi}\operatorname{acosh}\left(\frac{s}{2r_W}\right) \quad [H/m]$$

Impedance per Unit Lenght

Two conductors AWG20 (26x34) at 2 mm distance (copper): l_e » 567 nH/m, r_{BF} » 26 mW/m



Parasitic Components of a Capacitor



R_s = series resistance (ESR)
R_p = parallel resistance
L = series inductance (ESL)

$$Z(jw) = R_s + jwL + \frac{R_p}{1 + jwR_pC}$$

Parasitic Inductor

$$L = L_s + L_i + L_w$$

L_s = inductance of the wound structure
L_i = inductance of internal leads
L_w = inductance of connecting wires

$$L_w = 2 l_w \left(\ln\left(\frac{4 l_w}{d_w} \right) - 1 \right) 10^{-7} \quad [H]$$

l_w = lenght of connecting wires [m]
d_w = diameter of connecting wires [m]

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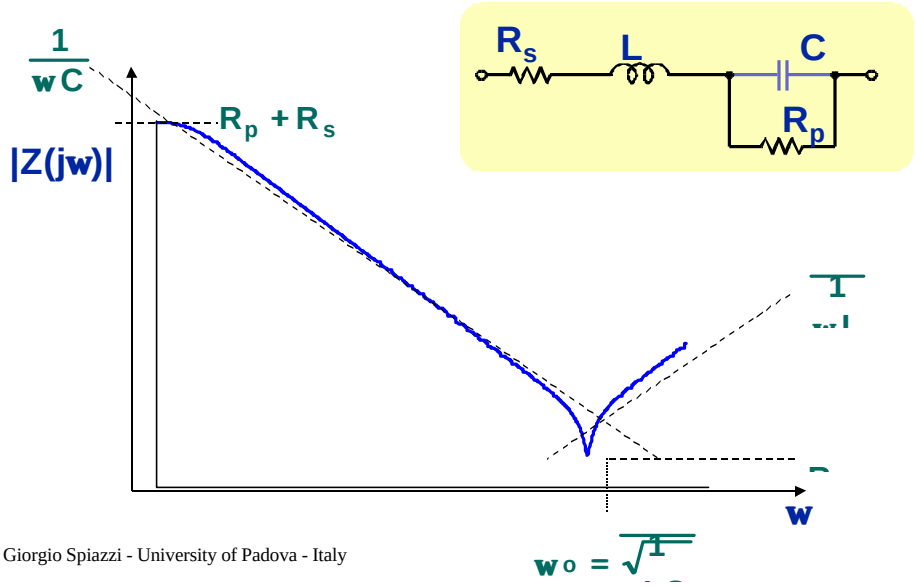
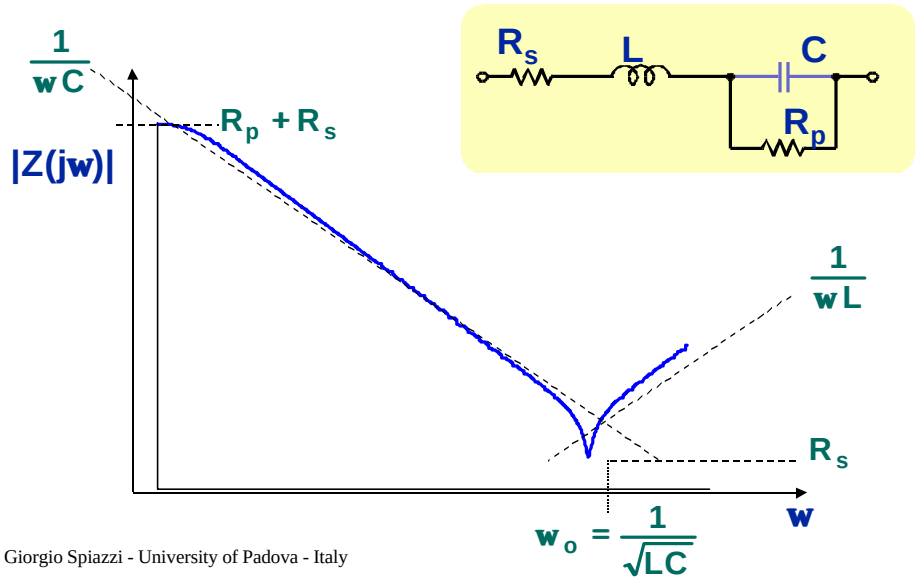
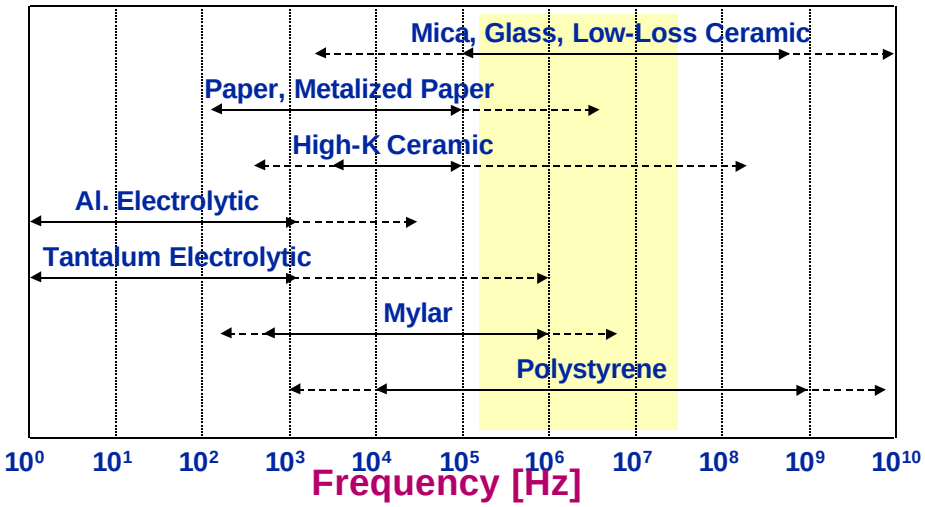
Impedance of a "Real" Capacitor



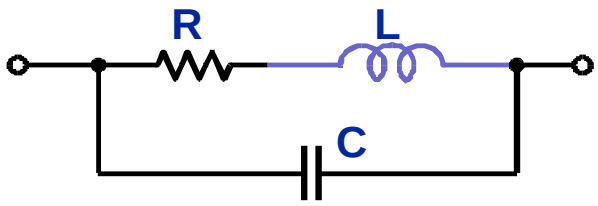
Impedance of a “Real” Capacitor



Approximate Usable Frequency



Parasitic Elements of an Inductor

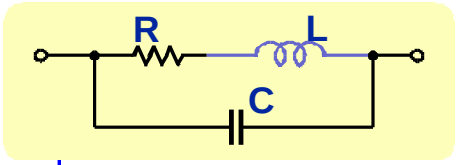


R = series resistance

C = parallel capacitance

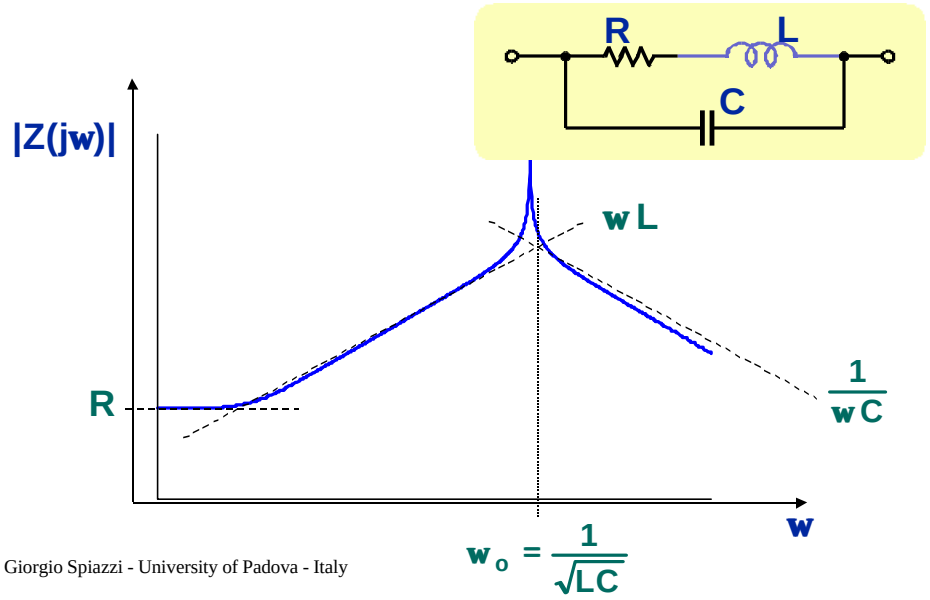
$$Z(jw) = \frac{R + jwL}{1 + jwRC - w^2LC}$$

Impedance of a "Real" Inductor



$w_o = \sqrt{\frac{1}{}}$

Impedance of a "Real" Inductor



$$w_o = \frac{1}{\sqrt{LC}}$$

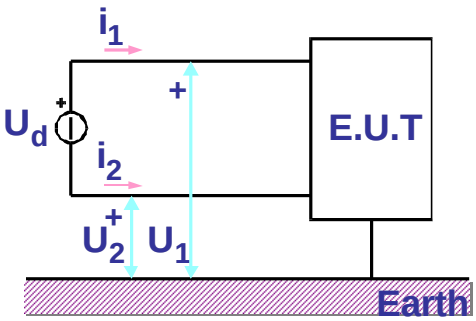
EMI Common Sources

- **Electronic circuits**
  - *Diode recovery*
  - *Switching components (SCR, IGBT, MOS)*
  - *Driving current pulses*
  - *Digital gates*
- **Magnetic components**
  - *Transformers*
  - *Inductors*
- **Circuit layout**
  - *High dv/dt in long wires*
  - *High di/dt in wide loops*
  - *High current wires*
- **Mechanical switches**
  - *relay (bounces, sparks, inrush currents*

Conducted Mode Signals

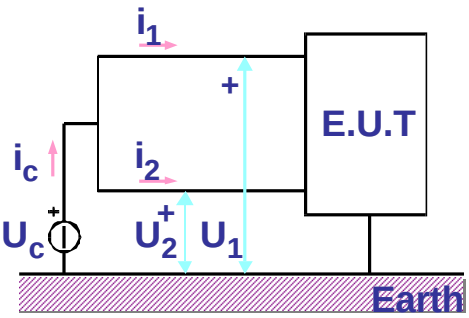
Differential mode

$$U_d = U_1 - U_2, \quad I_d = \frac{I_1 - I_2}{2}$$



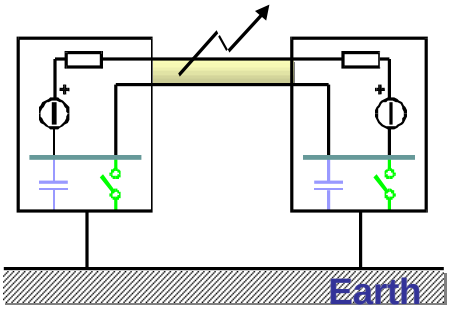
Common mode

$$U_c = \frac{U_1 + U_2}{2}, \quad I_c = I_1 + I_2$$

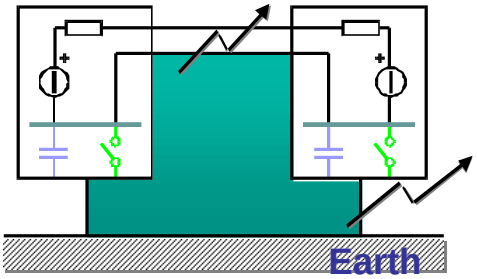


Radiated Signals

Differential mode

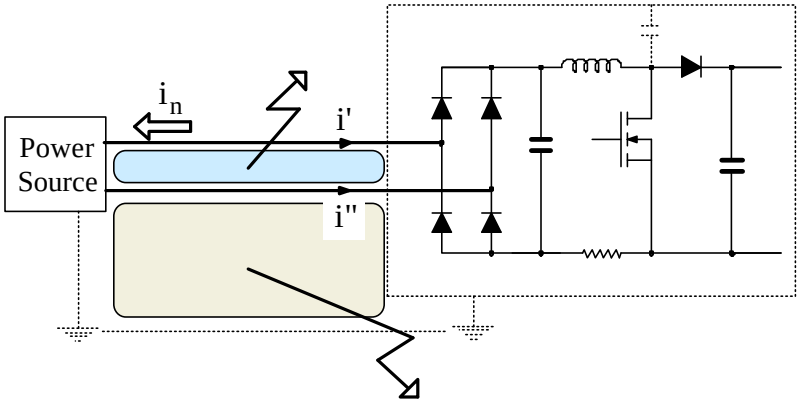


Common mode



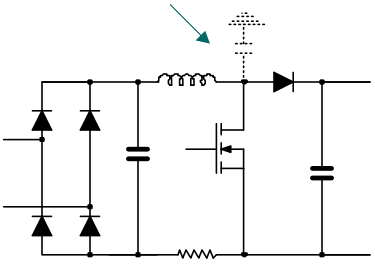
Example of Radiated Signals

Boost rectifier

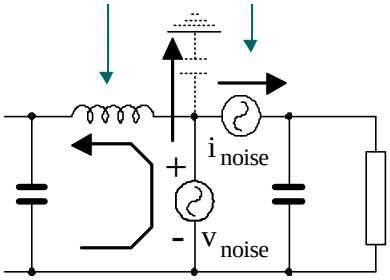


Conducted Noise

Common mode: parasitic capacitances between AC hot traces and chassis



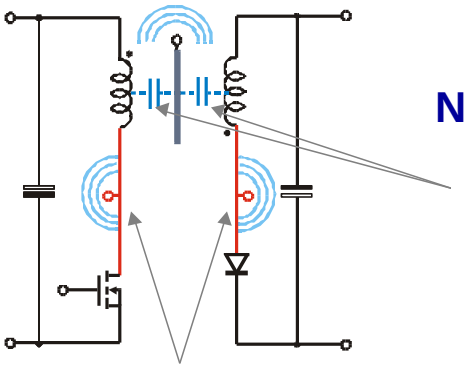
Differential mode: current ripples and spikes



- Switching devices can be seen as noise generators impressing noise voltages or injecting noise currents in the circuit
- Filters and parasitic elements must be taken into account in order to determine noise current and voltage amplitudes

Radiated Electric Field

Parasitic capacities to free space

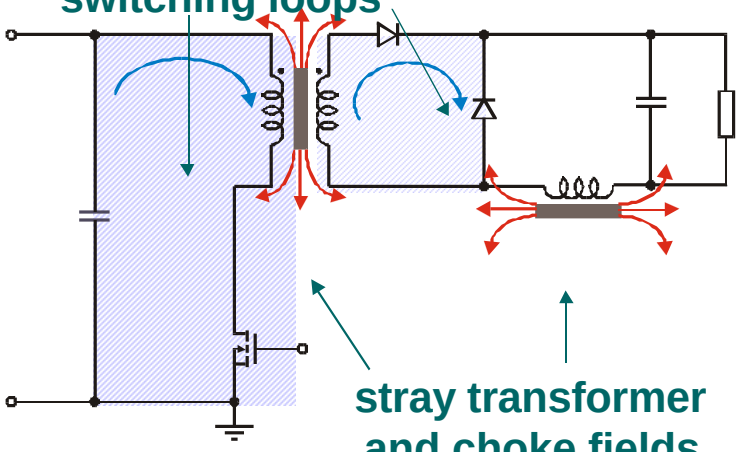


Noise coupled to core through winding-core capacitances

AC hot traces

Radiated Magnetic Fields

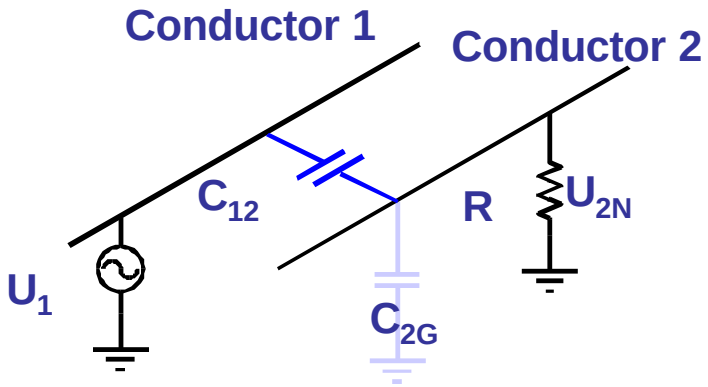
Typical input and output switching loops



stray transformer and choke fields

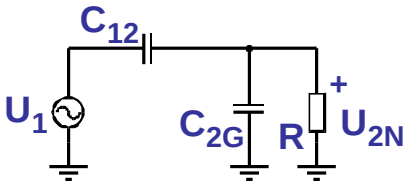
Capacitive Coupling

C_{12} = parasitic capacitance between conductors 1 and 2



Capacitive Coupling

Equivalent circuit

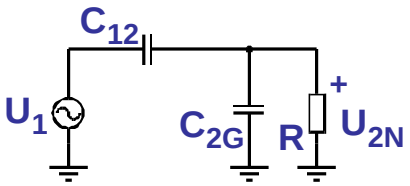


Voltage noise U_{2N} induced in conductor 2

$$\frac{U_{2N}}{U_1} = \frac{jw}{jw + \frac{1}{R(C_{12}+C_{2G})}} \times \frac{C_{12}}{C_{12}+C_{2G}}$$

Capacitive Coupling

Equivalent circuit



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Capacitive Coupling

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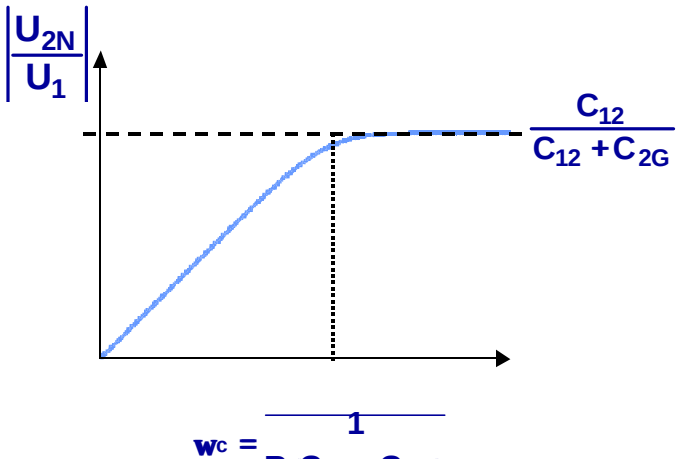
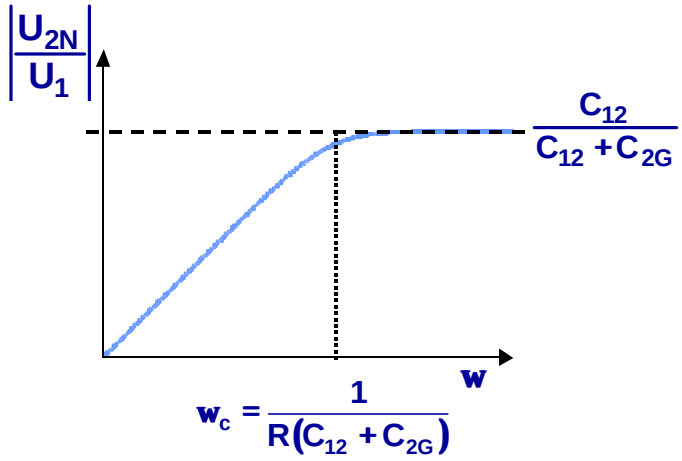


$$w_c = \frac{1}{\quad}$$

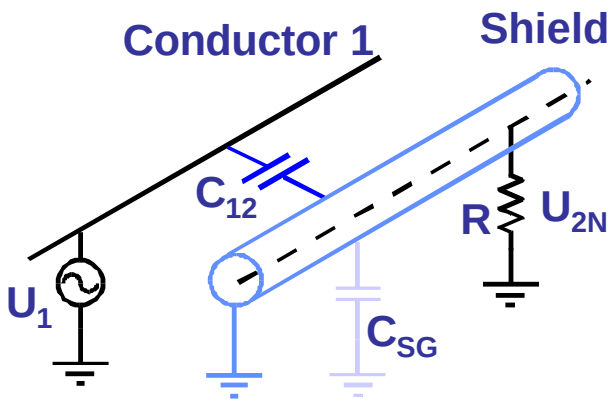
Capacitive Coupling

Voltage noise U_{2N} induced in conductor 2



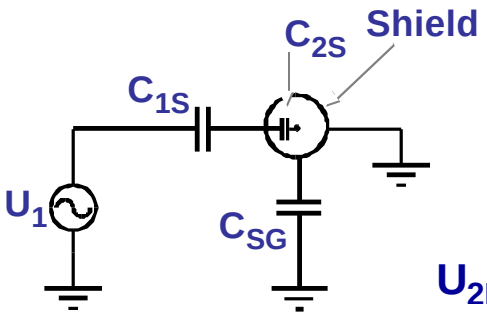
Capacitive Coupling

Grounded shield



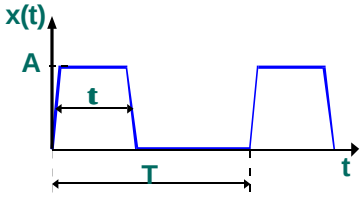
Capacitive Coupling

Grounded shield

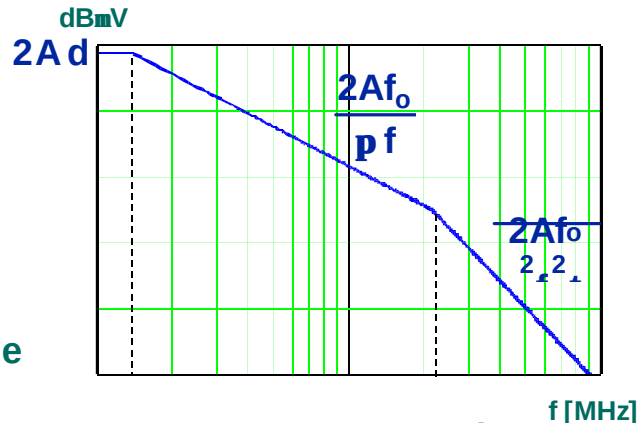


$U_{2N} = 0$

Spectrum Envelope of a Trapezoidal Periodic Signal

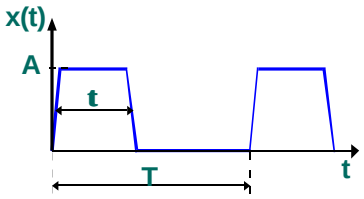


$d = \frac{t}{T}$ duty - cycle

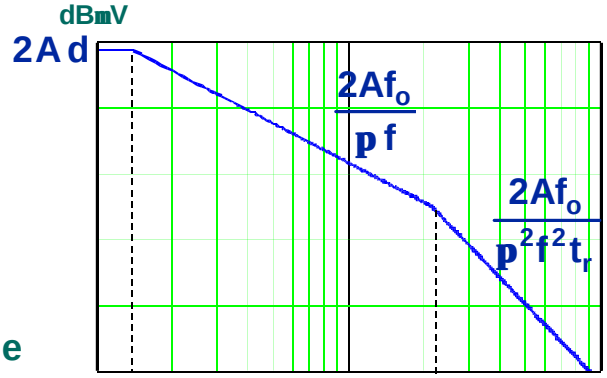


$f_1 = \frac{1}{\pi t}$ $f_2 = \frac{1}{\pi t}$

Spectrum Envelope of a Trapezoidal Periodic Signal



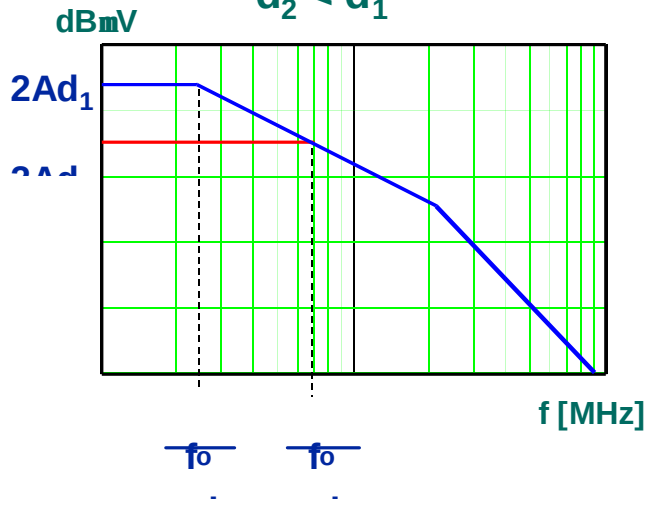
$$d = \frac{t}{T}$$ duty - cycle



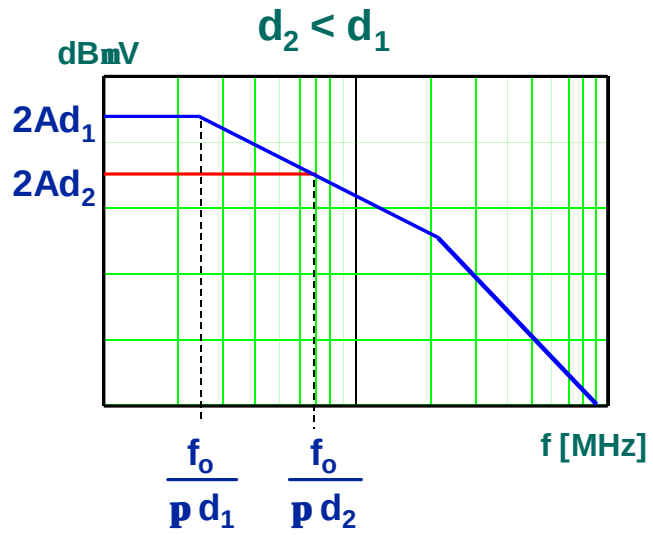
$$f_1 = \frac{1}{\pi t}$$ $$f_2 = \frac{1}{\pi t_r}$$

Effect of Duty-Cycle Variations

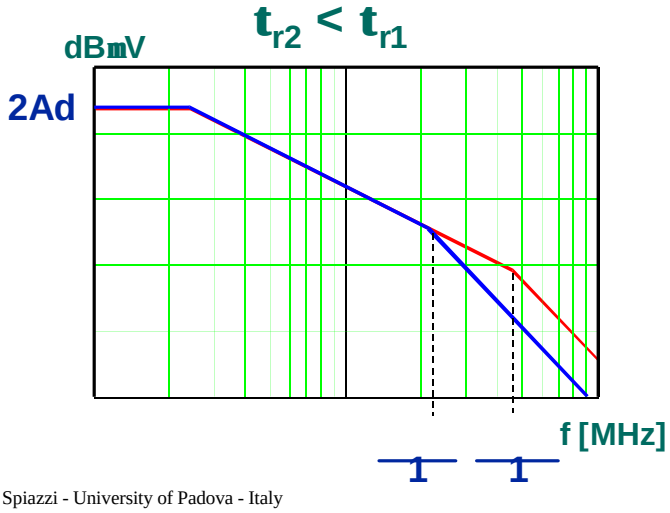
$d_2 < d_1$



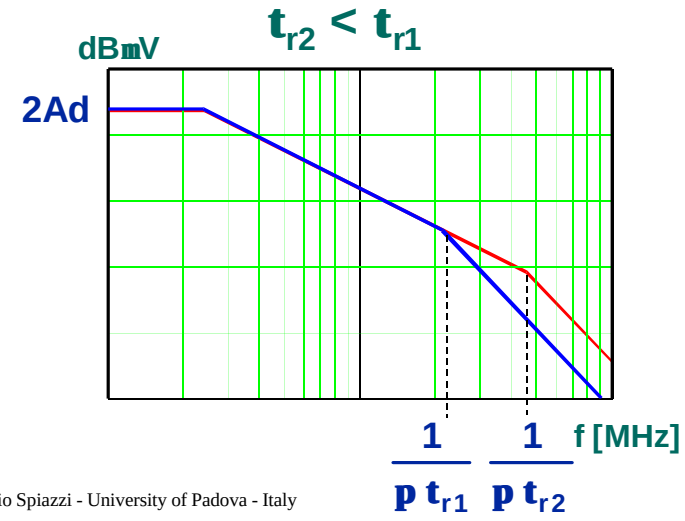
Effect of Duty-Cycle Variations



Effect of Rise and Fall Time Variations

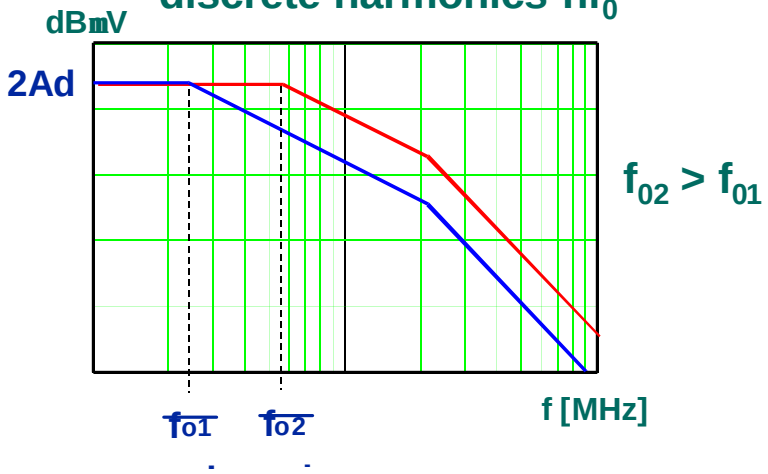


Effect of Rise and Fall Time Variations



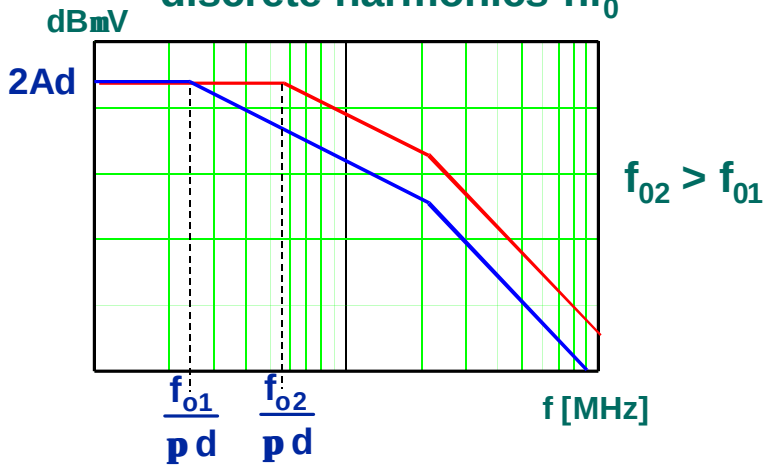
Effect of Repetition Frequency Variations

NOTE: change the distance between discrete harmonics nf_0

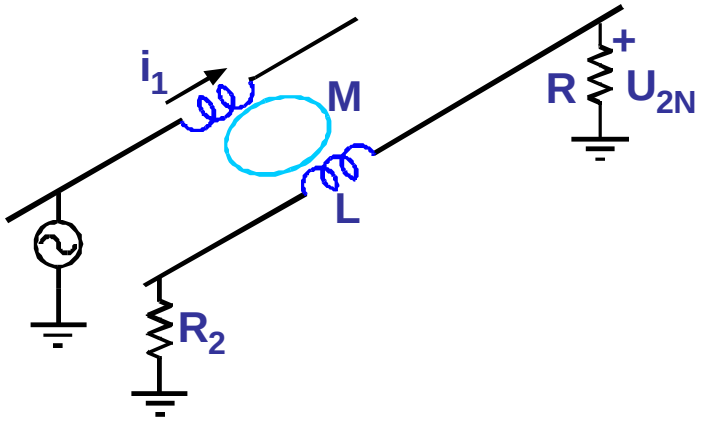


Effect of Repetition Frequency Variations

NOTE: change the distance between discrete harmonics nf_0

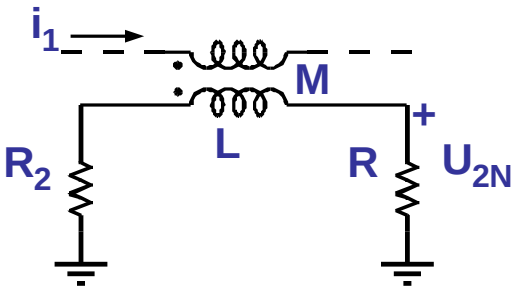


Inductive Coupling



Inductive Coupling

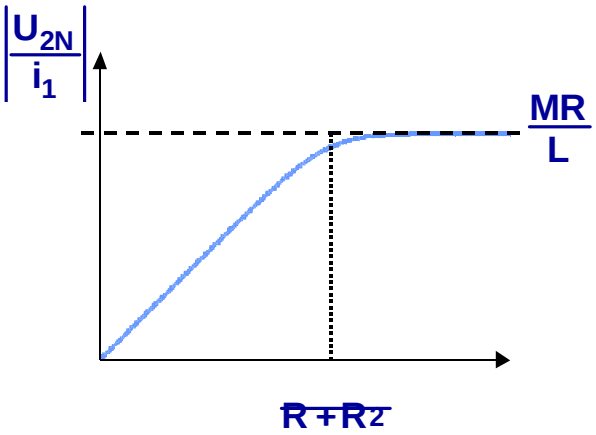
Equivalent circuit



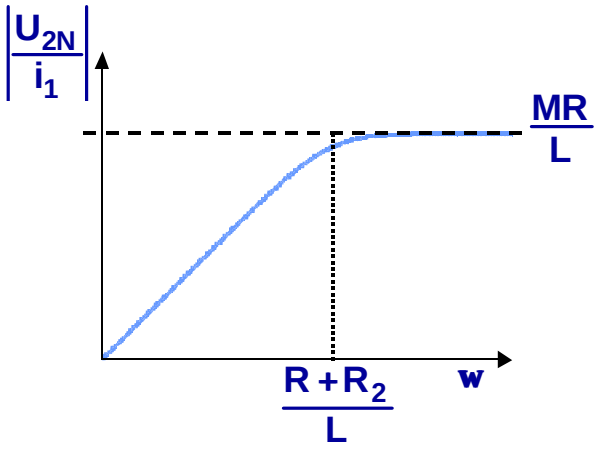
Voltage noise U_{2N} induced in conductor 2

$$\frac{U_{2N}}{i_1} = \frac{jw}{jw + \frac{R + R_2}{L}} \times \frac{MR}{L}$$

Inductive Coupling

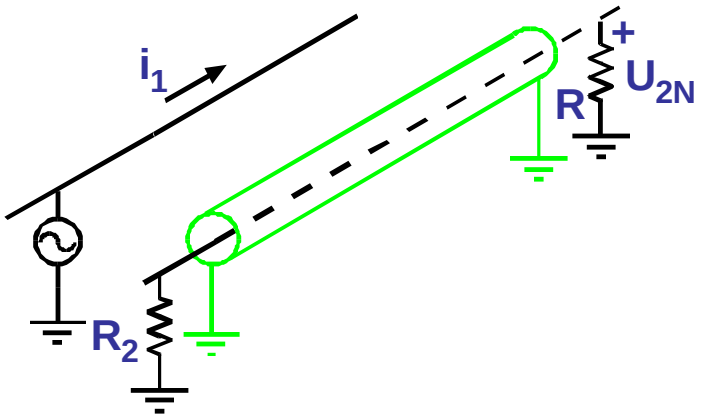


Inductive Coupling



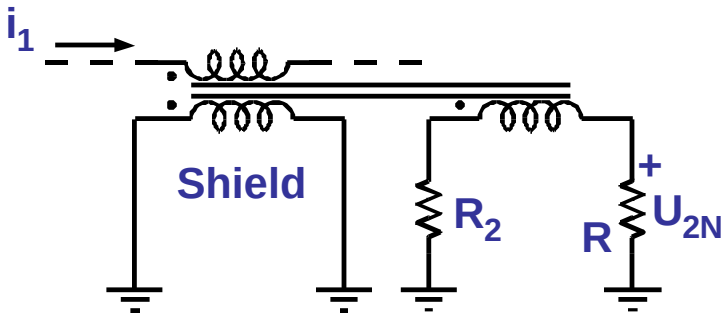
Inductive Coupling

Shield grounded at both ends



Inductive Coupling

Shield grounded at both ends



Shield acts as a short-circuited transformer secondary

Chassis Ground

- Also often a "safety ground"
- Includes metallic chassis, framework, etc.
- Often tied to a true "earth"
- As a rule, not used as a power return conductor (except in some low-voltage DC applications, like autos)
- Also common mode conducted noise return

Circuit Ground

- Usually refers to "circuit common"
- May be connected to chassis ground, but is best considered as separate and isolated during design
- Often the negative rail in DC systems, but the positive voltage rail may also be used

AC Quiet Rail

- Also known as AC LOW or RF LOW
- Used for local HF bypassing in EMI control
- Typically one of the DC or LF AC supply rails
- Not necessarely the same as circuit common

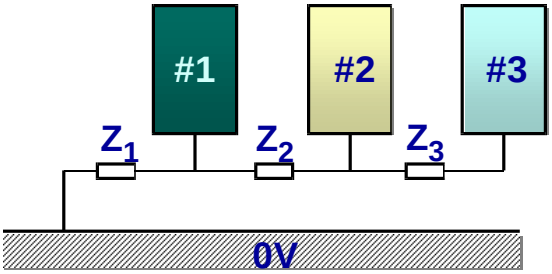
Ground Plane

A large metallic area (typ. on a PC board), which serves as:

- Magnetic field reduction through image currents
- Electrostatic faraday shield
- Circuit common / power return
- AC quiet rail
- Thermal Heat spreader
- Printed circuit board stiffening
- Typically not connected to chassis ground, but may be in some cases (usually undesirable for EMI)

Single-Point Grounding

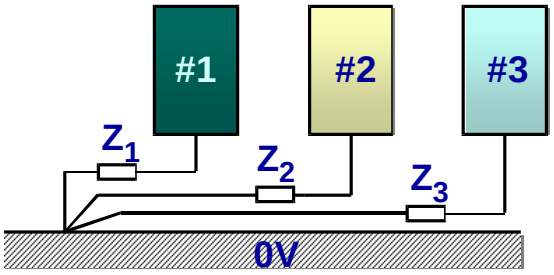
Series connection



The most sensitive circuit must be closest to the physical ground point (#1)

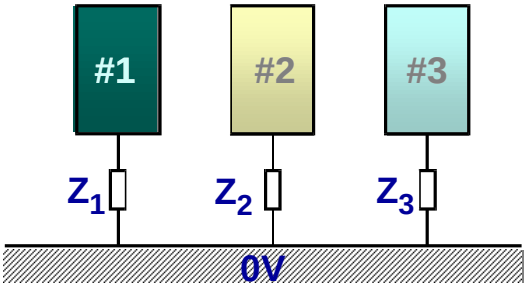
Single-Point Grounding

Parallel connection



Difficult at high frequency (long connections)

Multiple Ground Points



Ground connection is minimized

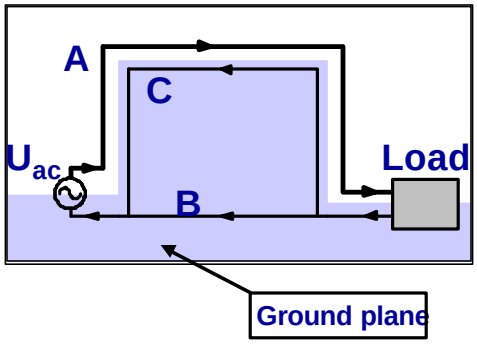
Ground Plane as Return Current Conductor

A - Signal path

B - Shortest low-frequency return path (smaller resistance)

C - Shortest high-frequency return path (smaller inductance)

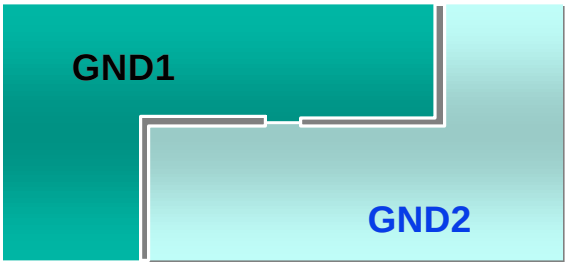
Different current components follow different return paths



- **Voltage drop on ground paths can be significant for high amplitude and high-frequency currents**
- **Actual current path is that with lowest impedance**
- **Ground planes are preferable in high frequency applications**

Ground Plane Separation

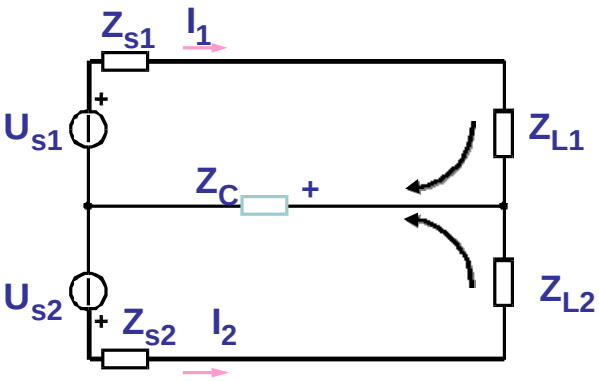
Return currents of each circuit remain separated



Common Impedance Coupling Path

$$U_{s1} = (Z_{s1} + Z_{L1} + Z_C) I_1 + Z_C I_2$$

Noise Voltage



Magnetic/Inductive Coupling Design Considerations

- Parasitic inductance is reduced with:
  - learger or wider conductors
  - smaller conductor spacing (lower magnetic field volume and energy)
- Magnetic field is reduced with:
  - magnetic shielding (high permeability or conductive)
  - generation of quadrapole (or higher order) fields with ground planes (image currents), twisted wires, etc.

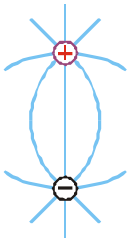
Magnetic Field Reduction with a Ground Plane

- Effect much higher behind ground plane
  - front: reduction due to image currents (quadrapole effect)
  - rear: eddy current field cancellation
- Ground plane slits and slots under conductors greately reduce its effectiveness
- Thin solid ground plane better than thick planes with slits or slots

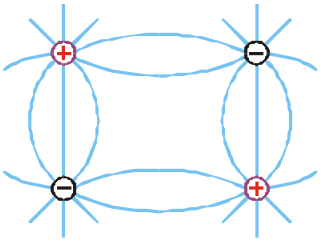
Far Field Intensity

Monopole field:
Field intensity μ $1/R^2$

Dipole field:
Field intensity μ $1/R^3$

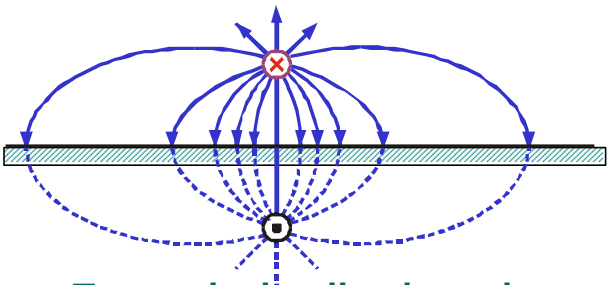


Quadrapole field:
Field intensity μ $1/R^4$



Ground Plane Effect

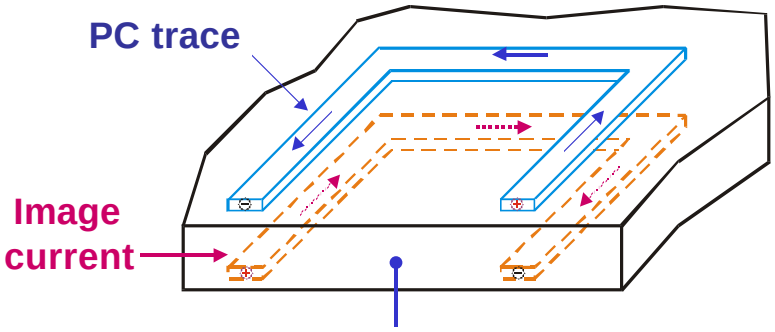
E and H fields distribute themselves as if a mirror image conductor existed at the opposite side of the ground plane, with an equal current in the opposite direction



Ground plane

Transmission line impedance Z_o is half of "imaged" line impedance

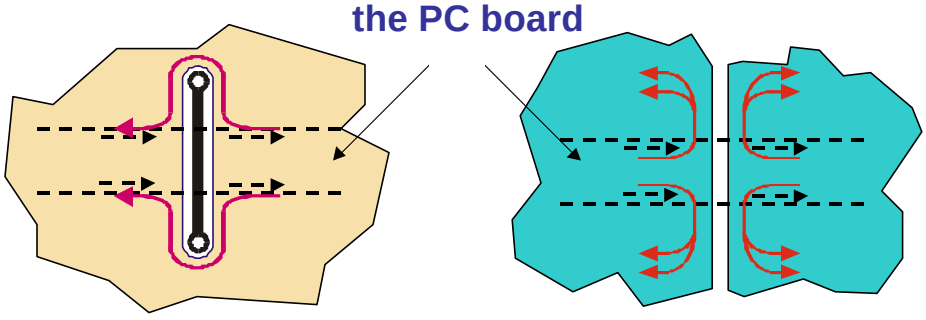
Magnetic Field Reduction with a Ground Plane



Counter-flowing image currents caused by a ground plane create a quadrapole magnetic field

Imperfections in the Ground Plane

PC trace on the other side of the PC board



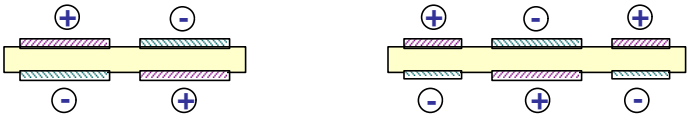
An open path in the ground plane creates a "slot antenna"

A break in the ground plane further reduces image current effect

Printed Circuit Power Conductors

Patterns for magnetic mid and far field intensities

Best, but usually not practical



Very good, sometimes practical

Printed Circuit Power Conductors

Patterns for magnetic mid and far field intensities

Quite good, usually practical for standard practice

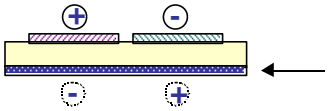


Image currents

Acceptable, due to quadrapole field from ground plane

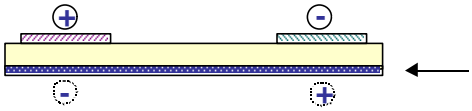
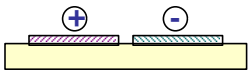


Image currents

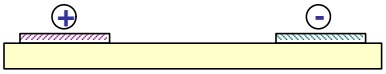
Printed Circuit Power Conductors

Patterns for magnetic mid and far field intensities

Poor, large dipole field and high AC losses due to current concentration on adjacent edges

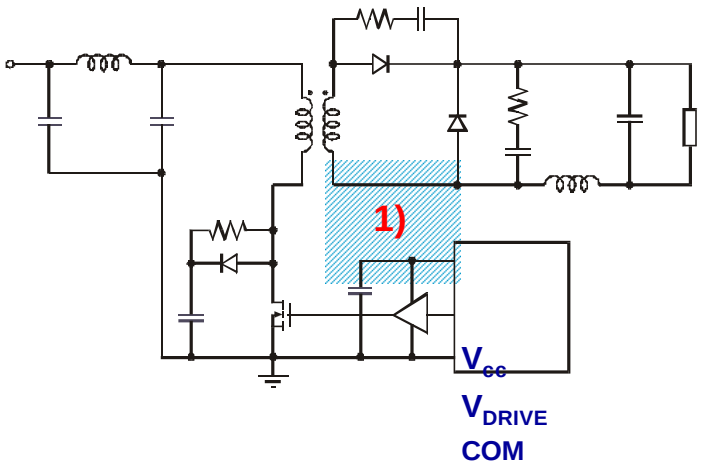


Unacceptable, very large dipole field (lower AC losses than the previous pattern)



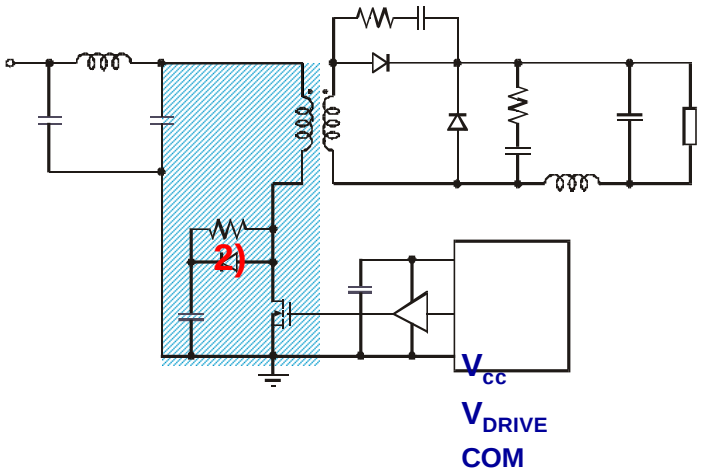
High di/dt Loops in a Forward Converter

1) Output transformer secondary - rectifier loop



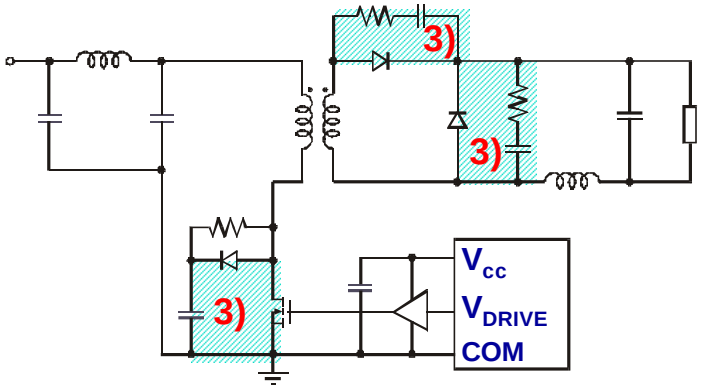
High di/dt Loops in a Forward Converter

2) Input switch-primary-bypass capacitor loop



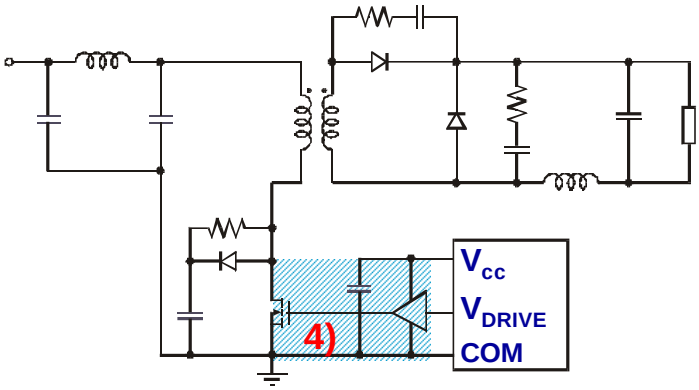
High di/dt Loops in a Forward Converter

3) Snubber loops on output rectifiers and input switches



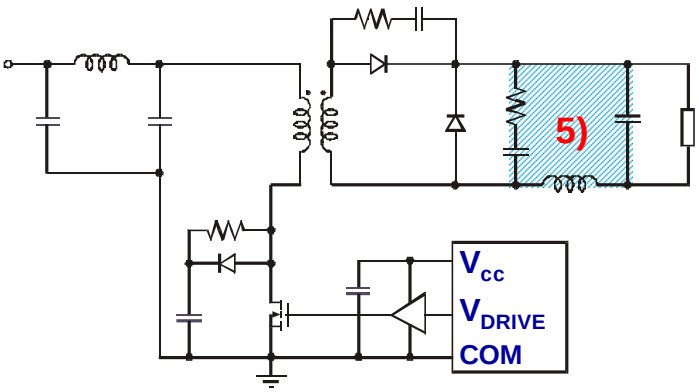
High di/dt Loops in a Forward Converter

4) Switch drive loops



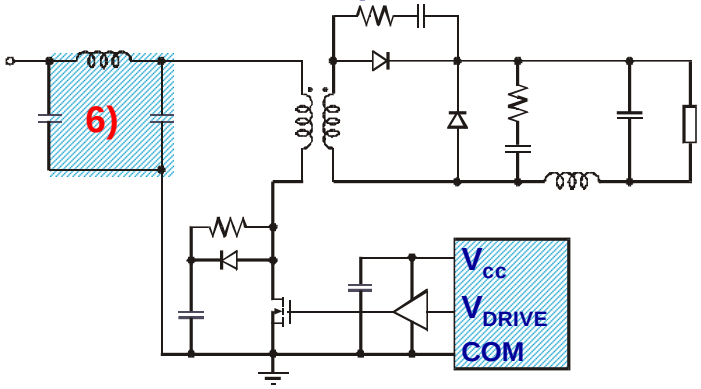
High di/dt Loops in a Forward Converter

5) Output filter inductor-capacitor loops



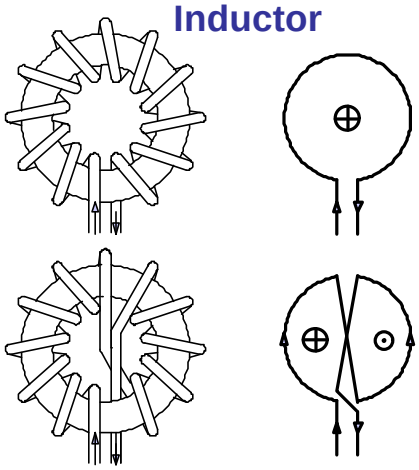
High di/dt Loops in a Forward Converter

6) Logic and control circuit loops, input filter loops

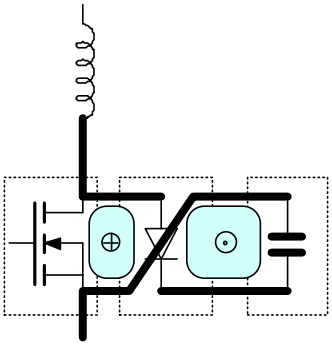


Avoiding Loop Antennas

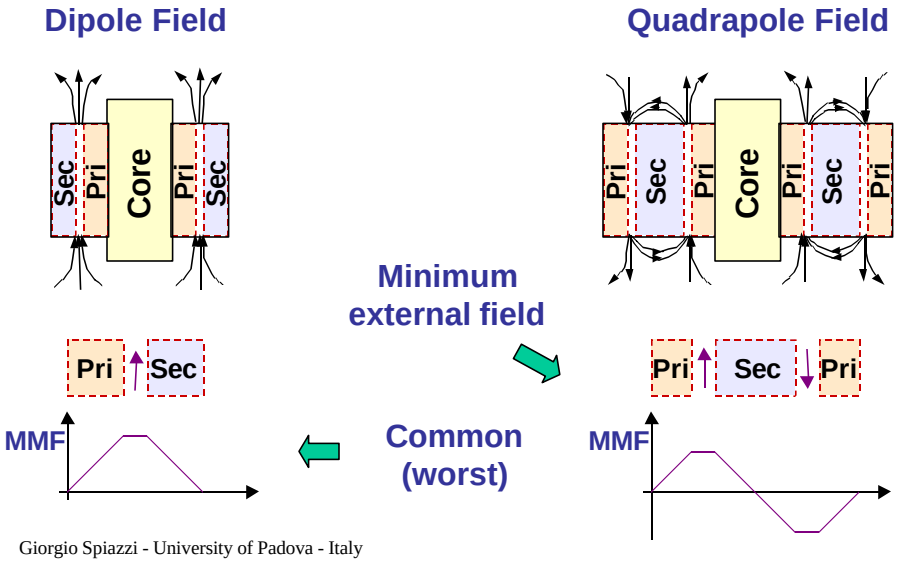
Ring core Inductor



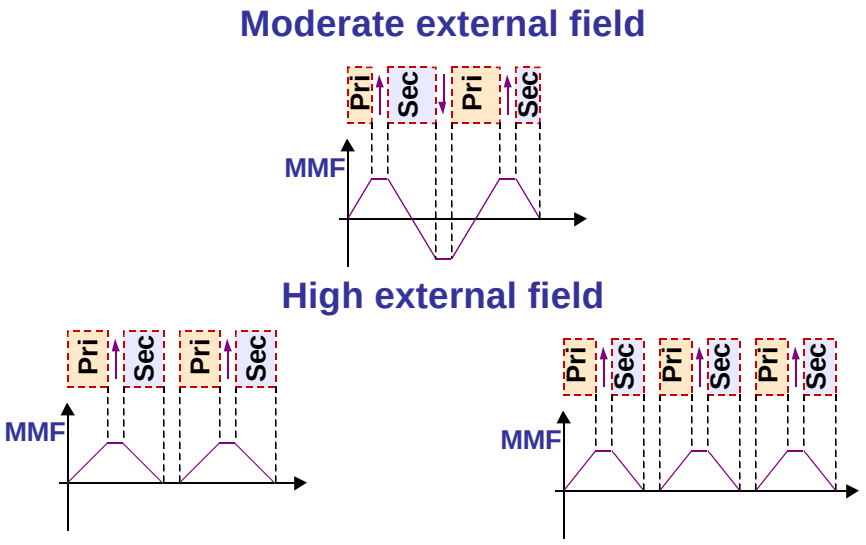
Snubber component layout



Transformer External Leakage Field



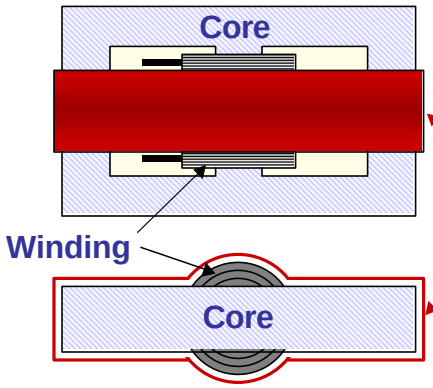
Transformer External Leakage Field



Shielding High-Frequency Magnetic Field

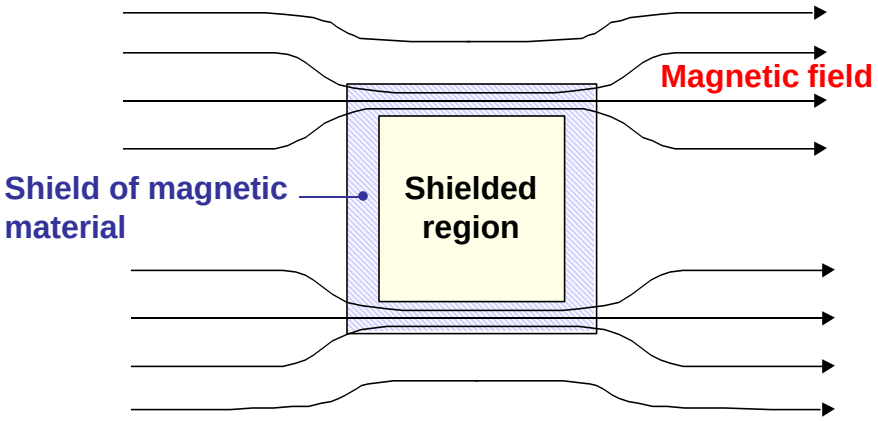
- Using short circuit loops to generate an opposing magnetic field

Example: transformer



Shielding Low-Frequency Magnetic Field

- Providing a low-reluctance magnetic path to divert the field around the circuit being protected



Magnetic Field Minimization

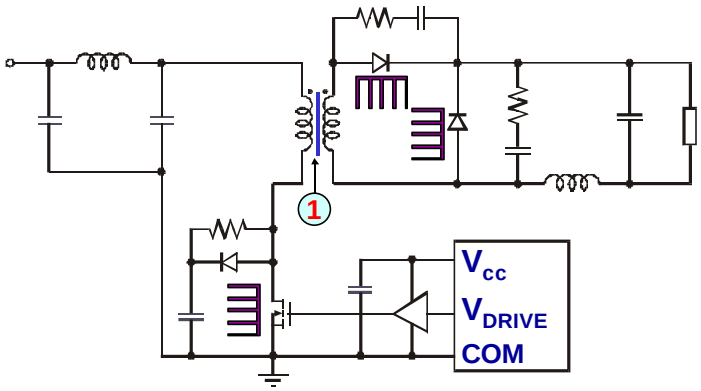
- Minimize leakage fields from transformer
  - use a sandwiched winding construction
  - use an electromagnetic shield strap
- Minimize leakage fields from inductors
  - avoid external air gaps
  - use uniform windings on “powdered iron” type of toroidal cores

Electric/Capacitive Coupling Design Considerations

- Much easier to shield than magnetic field
- Electric field sources of EMI can be reduced by:
  - using power circuit topologies with low semiconductor case AC potentials
  - using power transformer electrostatic shields
  - bypassing power magnetic cores to AC quiet
  - minimizing AC hot conductors length and area, increasing spacing
  - using faraday shields (often ground plane)
- Conductor geometries which reduce mid and far fields also minimize external noise pickup

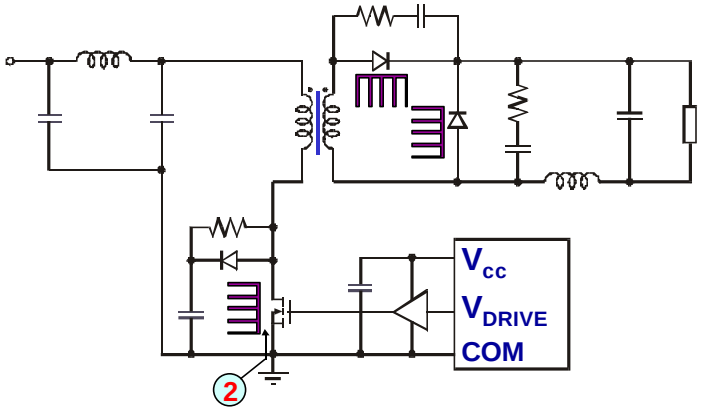
High dv/dt nodes in a Forward Converter

1) Transformer primary driving secondary and core (high node capacity)



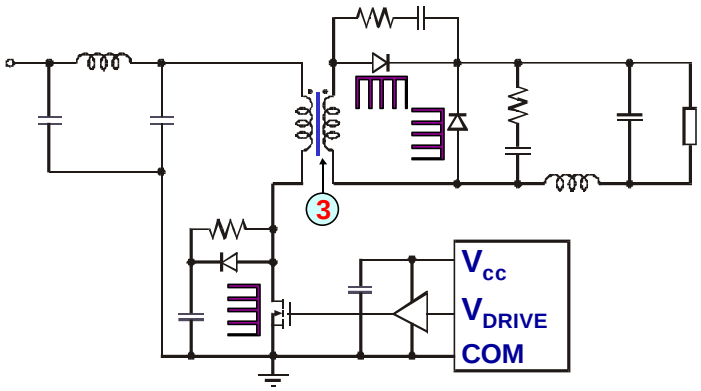
High dv/dt nodes in a Forward Converter

2) Primary switch driving heat sink (high node capacity)



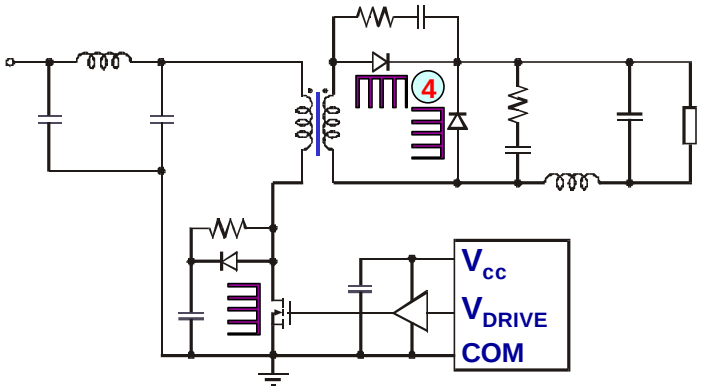
High dv/dt nodes in a Forward Converter

3) Transformer secondary driving primary and core (high node capacity)



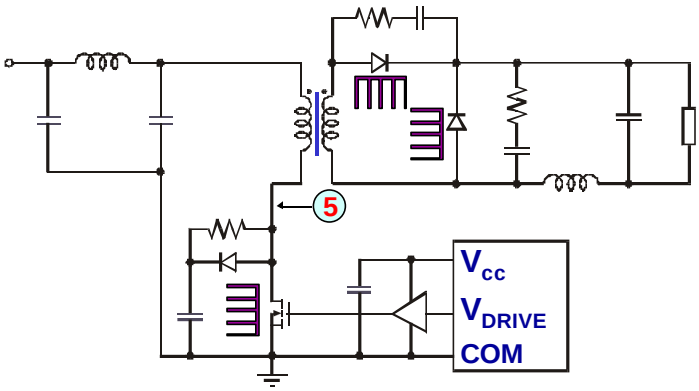
High dv/dt nodes in a Forward Converter

4) Rectifier cases driving heat sinks (high node capacity)



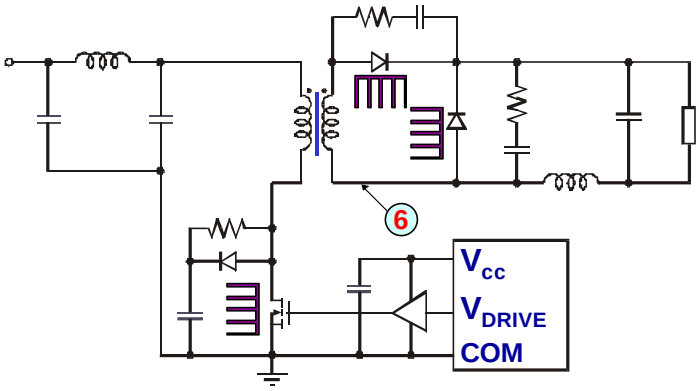
High dv/dt nodes in a Forward Converter

5) Primary switch “AC hot” PC trace



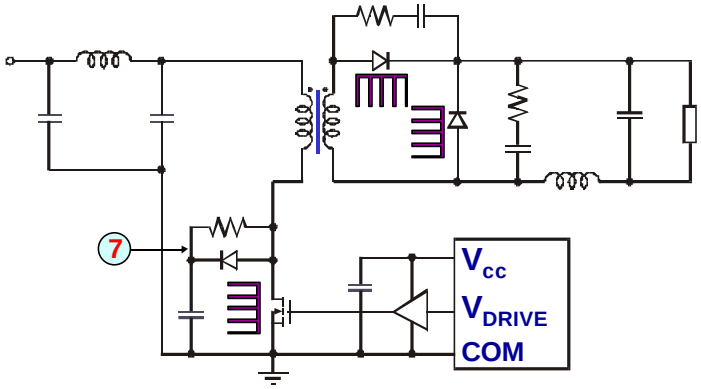
High dv/dt nodes in a Forward Converter

6) Output rectifier “AC hot” PC traces



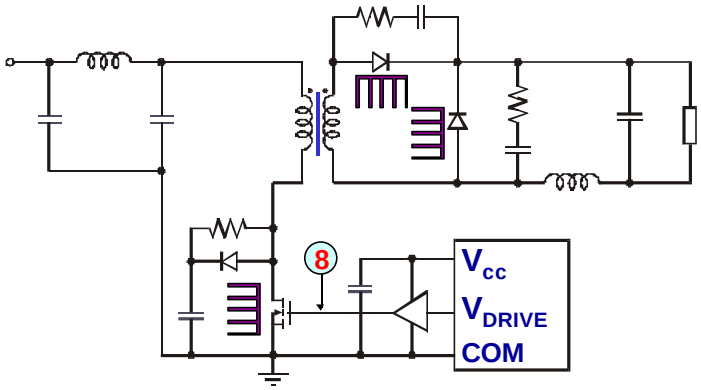
High dv/dt nodes in a Forward Converter

7) Snubber and clamp nodes, in some circuits



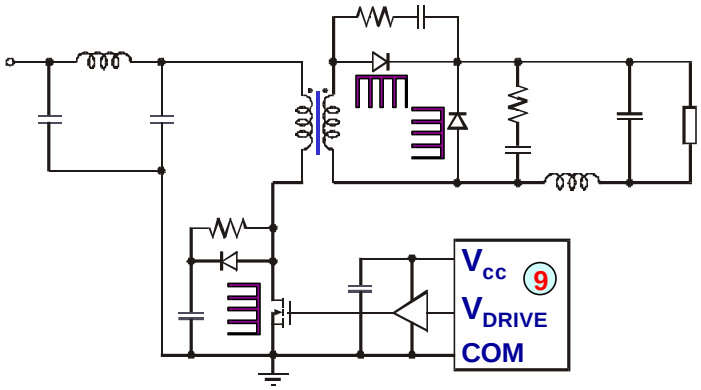
High dv/dt nodes in a Forward Converter

8) Switch drive (particolary FETs)



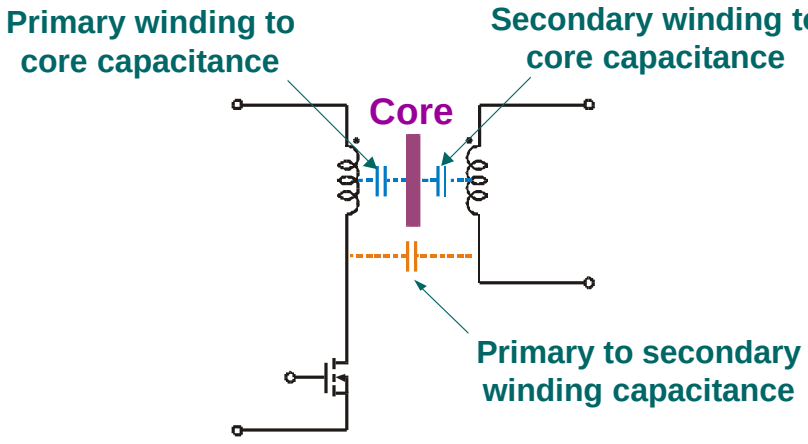
High dv/dt nodes in a Forward Converter

9) Digital logic traces



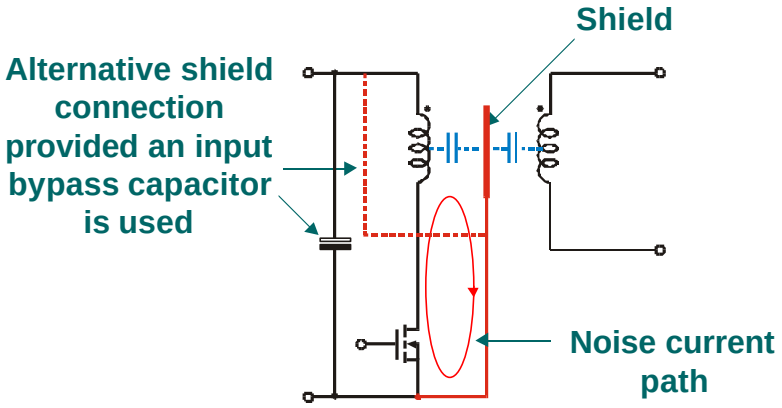
Electrostatic Shields in H.F. Transformers

Unshielded Transformer



Electrostatic Shields in H.F. Transformers

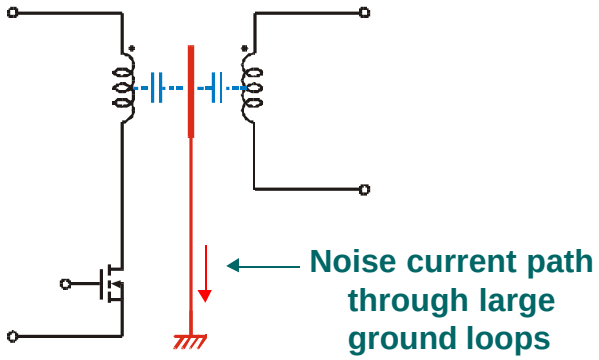
Shielded Transformer



Giorgio Spiazzi - University of Padova - Italy

Electrostatic Shields in H.F. Transformers

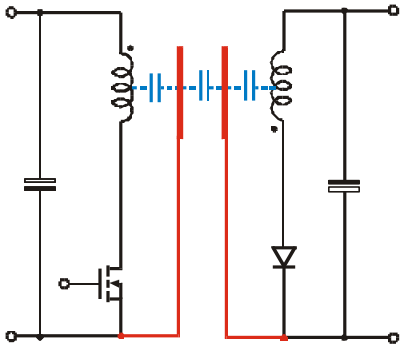
Incorrect shield connection



Giorgio Spiazzi - University of Padova - Italy

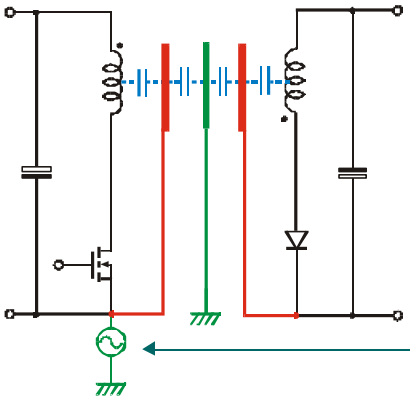
Electrostatic Shields in H.F. Transformers

Shielded Transformer: primary and secondary shield connections



Electrostatic Shields in H.F. Transformers

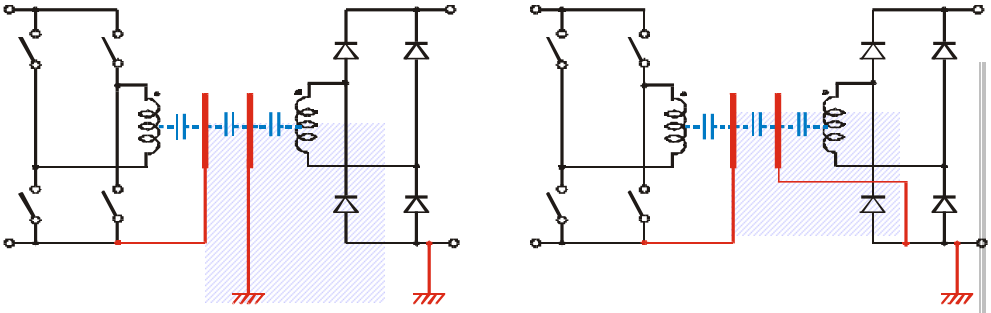
Shielded Transformer: a third grounded shield can now be used for safety and/or to minimize feedthrough of source common mode noise



Common mode
Noise source

Electrostatic Shields in H.F. Transformers

Check for shield current paths

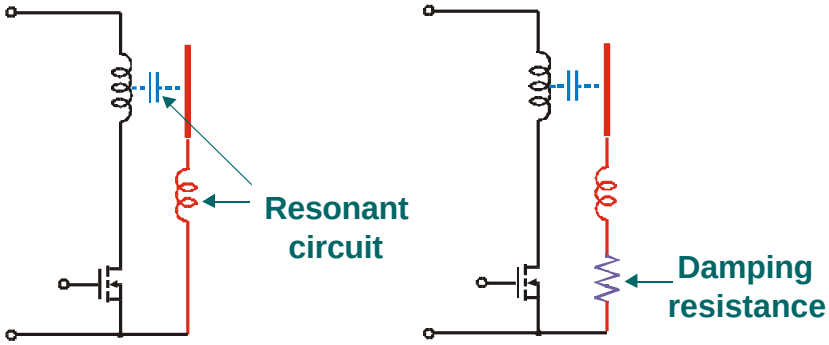


Large current loop and through ground

Small current loop not through ground

Electrostatic Shields in H.F. Transformers

Shield effectiveness at high frequencies is limited by shield capacity and lead inductance. Use a series resistance for damping



Electrostatic Shields Design Tips

Electrostatic shield should:

- form a full coverage, non-shorting turn
- have uniform insulation thicknesses
- consist of relatively thin and resistive material
  - 0.003” brass is generally suitable
  - down to 0.001” brass preferred at f > 1MHz
- be center tapped
- have a short drain wire connection, preferably foil closely spaced to foil winding breakouts

Common Mode Noise Minimization

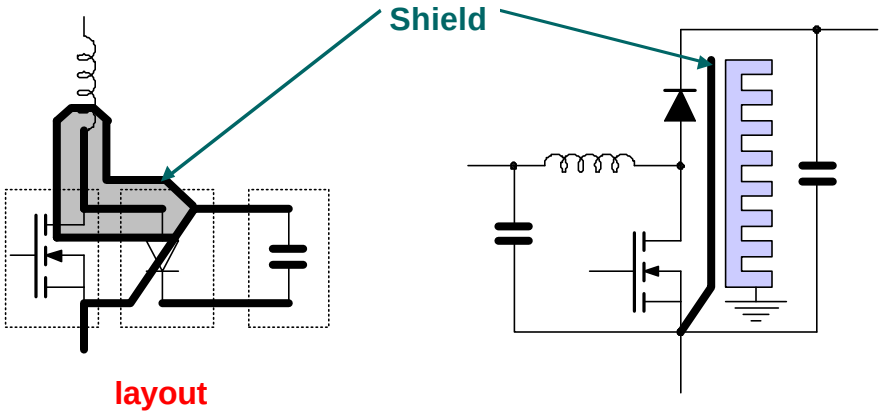
Minimize all sources of HF AC coupling to chassis

- Minimize AC hot traces on chassis side of PCB
- Use “common” traces to shield AC hot traces
- Avoid mointing AC hot cases on grounded heat sinks
- Tie power magnetic cores to AC quiet

Minimize all coupling of HF AC from input to output

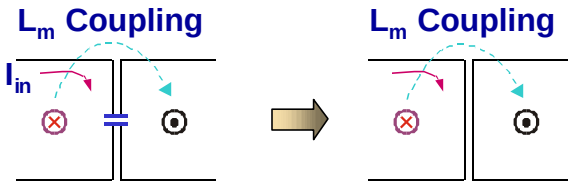
- Keep primary and secondary circuits well separated
- Nearest primary and secondary conductors should “commons”
- Use shields in isolation transformers

Shielding AC Hot Traces and Cases

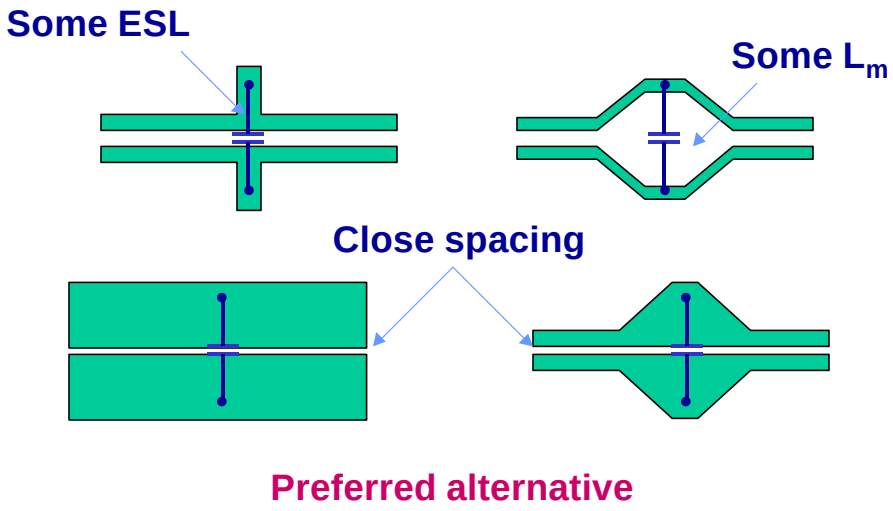


Connection of Capacitors

Mutual inductance coupling. The same L_m coupling occurs with shorted, isolated PC traces of the same geometry (typically 2-20 nH)



Connection of Capacitors



Preferred alternative

General Layout Considerations 1°

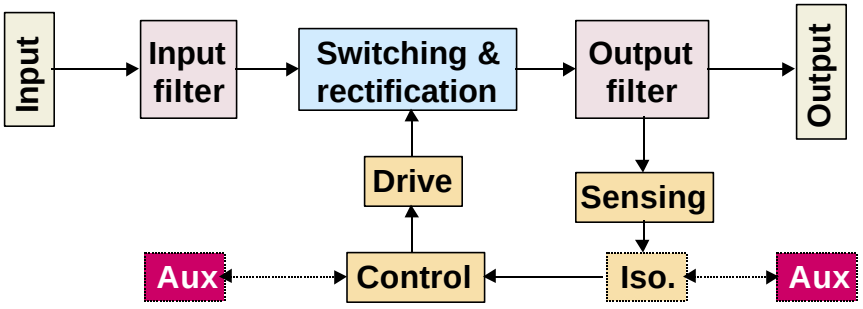
- In general, the power, drive, and logic physical layout should resemble a neat schematic
- Keep isolated circuits physically separated
- Keep noisy power circuits away from logic and low-voltage control circuitry
- Keep power switching circuits away from filtered inputs and outputs
- Place drivers close to switches and away from logic
- Parallel discrete or dual diodes with caution: different T_{rr} can excite HF oscillations

General Layout Considerations 2°

- Minimize component lead inductances
  - surface mount components are preferred
  - radial leaded components should be mounted normal to the PCB (i.e. standing up)
  - axial leaded components should be mounted parallel to the PCB (i.e. laying down)
  - keep leads as short as possible (ESL is proportional to lead length
- keep snubber and clamp loops as small and close to snubbed devices as possible

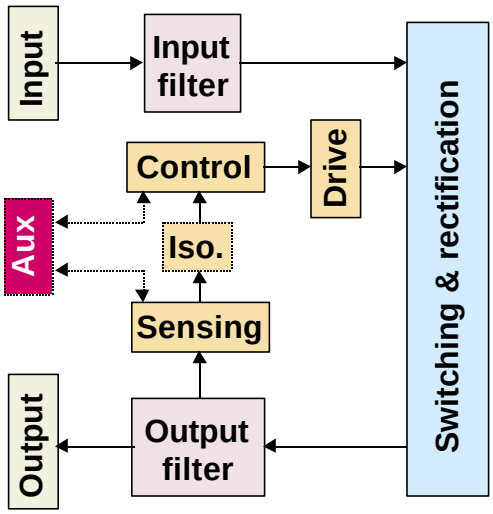
Linear Power Path

Minimize noise coupling from switching circuits into input and outputs



Folded Power Path 1°

Still good layout



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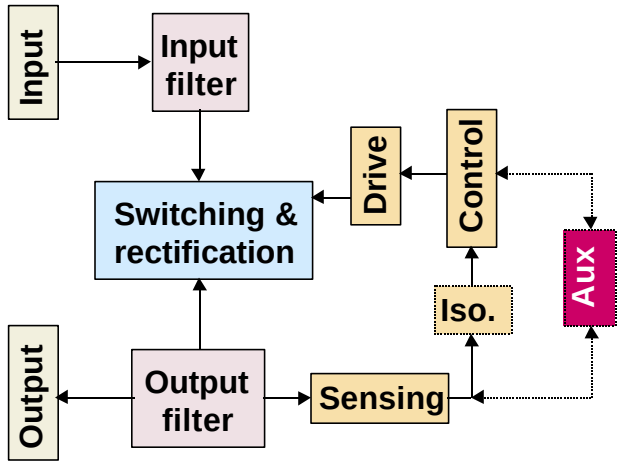
Folded Power Path 2°

Less desirable layout



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